Energy-efficient Nanocomputing Circuit by Multiferroic Nanomagnets

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Magnetoelastic switching in multiferroic nanomagnets with a small voltage is a promising substitute for current charge-based CMOS devices. Here, we study strain-mediated multiferroic majority logic gate by solving Landau-Lifshitz-Gilbert equation and establish an energy-efficient CMOS compatible equivalent circuit analogy to capacitor's I-V characteristics. We can easily simulate nanomagnet logic units using this tool. After that, the circuit is verified by SPICE simulations. Results show that the output voltage polarity is determined by the majority of input voltage polarity with ultralow energy consumption, working similarly to majority logic function. The SPICE circuit model shows ultralow energy consumption because of the conserved dynamic current, which can serve as a promising logic unit, consequently, integrated into large-scale nanomagnetic logic circuits and even a nanomagnetic chip.

Introduction: Nanomagnetic computing has attracted much attention due to its inherent non-volatile and energy-efficiency in next-generation computing technology[1]. The classical logic bits 0 and 1 are encoded into the stable magnetization direction of nanomagnets, which are parallel to the easy axis of the nanomagnet with large shape anisotropy. The digital information is propagated via magnetic dipole coupled interactions. This scheme increase the capacity of storage devices by one or two orders of magnitude. In view of these attractive characteristics, we believe that nanomagnetic logic devices may have great application prospects in the future, including intelligent magnetic field sensors, processing in memory architecture, and even complex signal processing units based entirely on magnetic field coupling. However, it needs an external energy supply(clock) to break shape anisotropy energy barrier during the propagation of information. One approach that transfers spin angular momentum to nanomagnets by injection of spin polarized current, known as spin transfer torque (STT), turns out to be dissipative due to I^2R[2]. To reduce energy dissipation, a much more energy-efficient way utilizing multiferroic nanomagnet is proposed[3, 4, 5, 6]. A tiny voltage applied across piezoelectric layer will generate stress transferred to magnetostrictive layer elasticly and rotate magnetization by a large angle. Logic computing can be designed by aligning nanomagnets properly [7, 8]. This concept is illustrated in Fig. 1, where a multiferroic majority logic gate is achieved by the dipole-dipole interaction between nanomagnets.

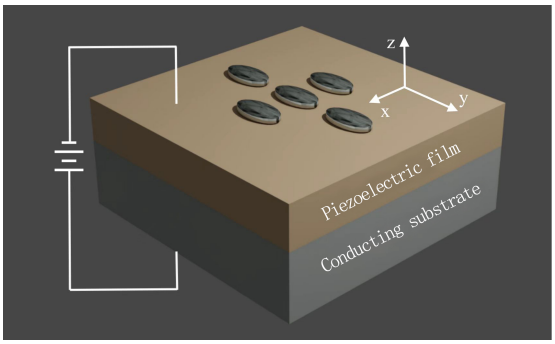


Fig. 1 *Multiferroic majority logic gate. The central nanomagnet works as a computing unit to determine the majority magnetization direction of 3 input nanomagnets.*

The mature micromagnetics theory describes the behavior of nanomagnet. However, this theory is too complex and computationally expensive to design large scale logic arrays. Therefore, researchers turned to SPICE macro model for simulating the interaction of nanomagnet arrays, which allows one to deal with these arrays embedded in microelectronic circuits. Csaba firstly introduced SPICE model as micromagnetic simulator, which based on the single domain approximation[9]. But their work seems enerey-inefficient because the nanomagnets are drived by magnetic field generated from charge current. Other researchers are concentrated on MTJ devices whose magnetic state is controlled through STT effect, thus, leading to a frustrating independent current source in SPICE model[10, 11, 12, 13, 14, 15, 16]. This eliminates the huge advantage of nanomagnets in power consumption. Xu established HSPICE circuit model of single strain-mediated multiferroic nanomagnet which works with ultralow energy dissipation[17]. Unfortunately, there is little research on the simulation of large scale logic circuits composed of multiferroic nanomagnets based on SPICE model.

A piece of work have been done on CMOS compatible circuit model of multiferroic majority logic gate employing voltage induced strain and the strong coupling interaction which shows a more energy-efficient scheme in future large scale nanomagnetic integrated circuits. We have demonstrated that it is possible to perform signal processing tasks using magnetic nanostructures, and that effective CAD tools can be developed to simulate nanomagnetic units. These results are of great significance to guide the design of nanomagnetic structure integrated into microelectronic circuits.

Spice Model of Multiferroic Majority Logic Gate:

Magnetization Dynamics

In this paper, we choose Terfenol-D as magnetostrictive material with a large positive magnetostriction coefficient $\lambda_s = 6 \times 10^{-4}$ and saturation magnetization $M_s = 8 \times 10^5$A/m. Elliptical nanomagnets of 101.75nm $\times$ 98.25nm $\times$ 10nm lateral dimensions have been fabricated on piezoelectric substrate with 40nm thickness as shown in Fig. 1. In this case, exchange coupling in nanomagnet prevents the formation of multi-domain states, so we can ignore the spatial change of magnetization in each magnetostrictive layer and model it as a single domain nanomagnet. In general, nanomagnets with a size of about 100nm show single domain behavior. The central one is a computing unit whose magnetization direction is determined by the majority of input nanomagnet magnetization. Temporal evolution of magnetization orientation is described by Landau-Lifshitz-Gilbert(LLG) equation under the influence of an effective field:

$$\frac{d\mathbf{M}}{dt} = -|\bar{\gamma}|\mathbf{M} \times \mathbf{H}_{\text{eff}} - \frac{|\bar{\gamma}|\alpha}{M_s}\mathbf{M} \times (\mathbf{M} \times \mathbf{H}_{\text{eff}}) \tag{1}$$

$\mathbf{M}$ is magnetization vector and α is Gilbert damping coefficient. $\bar{\gamma}$ is Landau-Lifshitz gyromagnetic ratio, mathematically equivalent to Gilbert gyromagnetic ratio form with the relation $\gamma = (1+\alpha^2)\bar{\gamma}$. $\mathbf{H}_{\text{eff}}$ is the effective magnetic field on any multiferroic element due to shape anisotropy energy, stress anisotrophy energy, dipole-dipole interaction energy[18]:

$$\mathbf{H}_{\text{eff}} = \mathbf{H}_{\text{dipole}} + \mathbf{H}_{\text{shape}} + \mathbf{H}_{\text{stress}} \tag{2}$$

We assume that the magnetostrictive layer is polycrystalline, so we can ignore the magnetocrystalline anisotropy. For the dipole coupled system, Eq. 1 can be rewritten as coupled ordinary differential equations by normalizing the magnetizaiton with respect to M_s:

$$\begin{aligned}
\frac{(1+\alpha^2)}{\gamma}\frac{dm_x}{dt} =& -\alpha(m_y(h_y m_x - h_x m_y) \\
& - m_z(h_x m_z - h_z m_x)) \\
& - (h_z m_y - h_y m_z) \\
\frac{(1+\alpha^2)}{\gamma}\frac{dm_y}{dt} =& -\alpha(m_z(h_z m_y - h_y m_z) \\
& - m_x(h_y m_x - h_x m_y)) \\
& - (h_x m_z - h_z m_x) \\
\frac{(1+\alpha^2)}{\gamma}\frac{dm_z}{dt} =& -\alpha(m_x(h_x m_z - h_z m_x) \\
& - m_y(h_z m_y - h_y m_z)) \\
& - (h_y m_x - h_x m_y)
\end{aligned} \tag{3}$$

where h_x, h_y, h_z are the components of the effective field and m_x, m_y, m_z are the components of normalized magnetization. Substitution of Eq. 3 in Eq. 2 allows us to compute the temporal evolution of the magnetization vector of any multiferroic element in the Fig. 1.

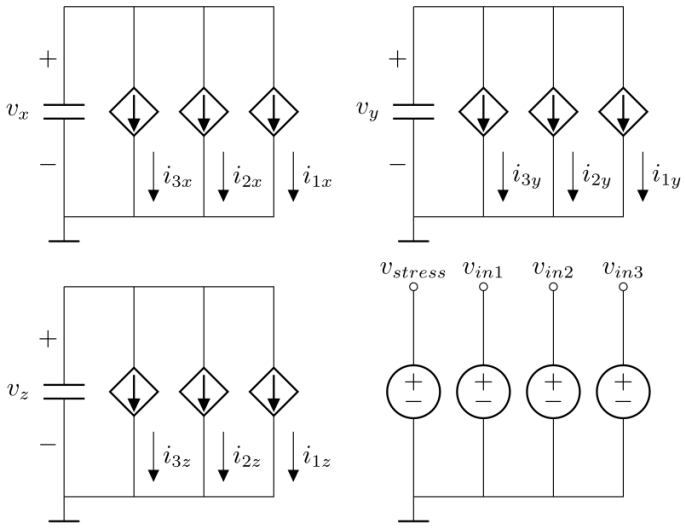


Fig. 2 *Schematic diagram of equivalent circuit of multiferroic majority logic gate.*

Equivalent Circuit Model

This part describes the majority logic gate model for circuit simulation using NGSPICE. Based on the single domain approximation, LLG subcircuit is developed to simulate the dynamic behavior of magnetization switching of multiferroic nanomagnet. This is accomplished by implementing Landau–Lifshitz–Gilbert equation with more energy efficient voltage induced strain.

According to the Kirchhoff current law and the I-V characteristics of capacitor:

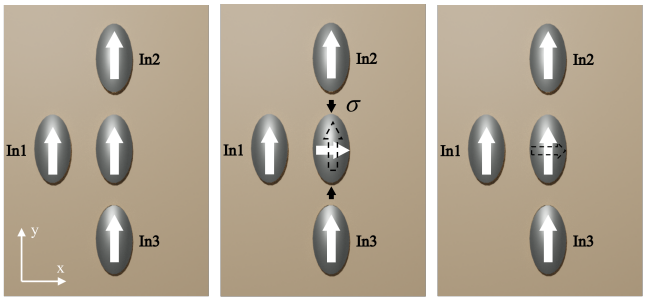
$$C\frac{dv}{dt} = \sum I_i \tag{4}$$

Assuming $m_x = v_x, m_y = v_y, m_z = v_z$, then the left-hand side of Eq. 3 can be seen as a capacitor with $C = (1+\alpha^2)/\gamma$ while the right-hand side can be seen as 3 parallel voltage controlled current source, each of them is related to some of m_x, m_y, m_z and $v_{in1}, v_{in2}, v_{in3}, v_{stress}$.

The CMOS compatible circuit model of multiferroic majority logic gate, shown in Fig. 2, is split into three subcircuits which models the magnetization switching behavior by the voltage polarity. Three independent voltage sources model the magnetization orientation of input nanomagnets while the dipole-dipole interaction strength between neighbors has been considered into the controlled current source by a additional distance parameter. V_{stress} models the stress anisotropy energy in magnetostrictive layer which depends on the materials parameters. It should be noted that the dipole-dipole interaction must be lower than shape energy barrier to prevent spontaneous magnetization switching but is still sufficient enough to ensure highly reliable magnetization switching after stress removal.

Spice Implementation of Multiferroic Majority Logic Gate: In this section, we will directly conduct circuit simulation using NGSPICE. Digital information is represented by magnetization component m_y. Logic "1" is assigned by $m_y = 1$ while logic "0" means $m_y = -1$. We assume that all nanomagnets are magnetized in the same direction in stage 1. During stage 2, the magnetization of output is erased by a considerable stress σ induced by a tiny voltage. In the stage 3, magnetization aligns automatically under the influence of neighbor nanomagnets after withdraw of stress. Indeed, the left nanomagnet (In1) prefers a downward magnetization direction while the other two prefer upward orientation when considering the coupling interaction. Therefore, output magnetization is determined by most of input willingness, working as a majority logic gate. The schematics of the logic operation are sketched in Fig. 3.

Corresponding SPICE simulation using a transient analysis of 20ns is shown in Fig. 4 and the initial value of v_x, v_y, v_z is set to 0.087V, 0.996V, 0.002V. The v_{stress} is taken to be -111mV, consequently, sufficient stress (about 40MPa) is transferred to magnetostrictive layer. In this circuit, v_y (represented by voltage of node 2) is equivalent to m_y. The voltage switching in circuit is similar to the magnetization switching behavior in nanomagnet. The value of 3 independent voltage



(a) Stage 1 (b) Stage 2 (c) Stage 3

Fig. 3. Operating principle for majority logic gate.

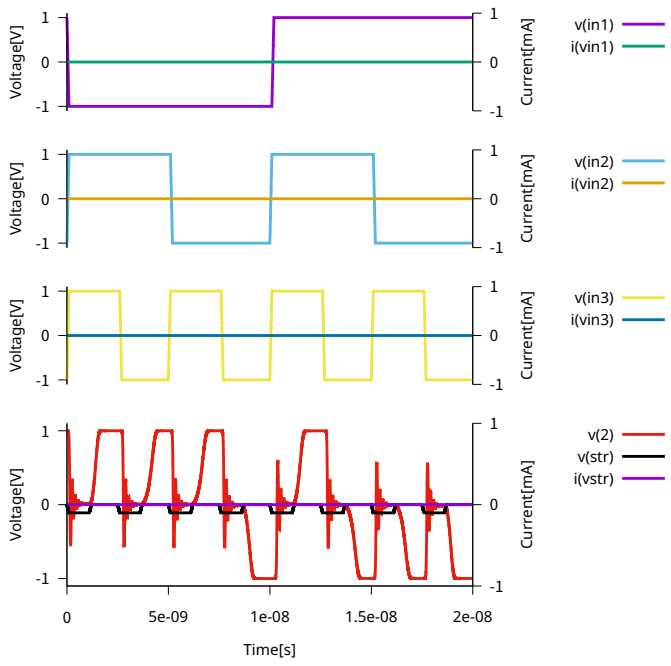


Fig. 4. SPICE simulation of multiferroic majority logic gate.

source means different input logic value. $v = 1$V is assigned to logic "1" while $v = -1$V means logic "0". During the every clock cycle, v_{stress} is applied to circuit with a duration of 1ns and v_2 changes to 0V as if the magnetization flipping to null state. After the withdraw of v_{stress}, v_2 is changed under the influence of $v_{in1}, v_{in2}, v_{in3}$ which is determined by the majority of $\bar{v}_{in1}, v_{in2}$ and v_{in3}, similar to the same logic computing of majority logic gate.

The current flow in independent voltage source is zero while the dynamic current in subcircuits is conserved due to the Kirchhoff current law. Therefore, the energy in circuit is mainly determined by the parasitic capacitance of piezoelectric layer, about $C_{piezo}V_{stress}^2 \approx 5194$kT[4] per switch while lacking of additional energy dissipated in reversing magnetization. This is a highlighted feature of SPICE model, which provides great convenience and superiority when conducting large-scale nanomagnetic circuits with a ultra low energy cost.

Conclusion: In this paper, we established a CMOS compatible circuit model of multiferroic majority logic gate by studying Landau-Lifshitz-Gilbert equation and utilized SPICE for solving micromagnetic problems. SPICE simulations show that voltage polarity switching is achieved which is similar to magnetization switching behavior. The interaction between nanomagnets is model by three independent voltage source, thus, changing voltage polarity in CMOS electronics is much more easier than switching magnetization in spintronics. We can use this equivalent circuit to achieve reliable logic function with a ultralow energy cost for digital information processing while signal propagation can be defined by proper placement of nanomagnets as before, consequently, shows

the feasibility of large-scale nanomagnetic integrated circuits and even a chip.

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References

1 R. P. Cowburn and M. E. Welland, "Room temperature magnetic quantum cellular automata," *Science*, vol. 287, no. 5457, pp. 1466–1468, 2000. [Online]. Available: https://www.science.org/doi/abs/10.1126/science.287.5457.1466

2 D. Ralph and M. Stiles, "Spin transfer torques," *Journal of Magnetism and Magnetic Materials*, vol. 320, no. 7, pp. 1190–1216, 2008. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0304885307010116

3 J. Atulasimha and S. Bandyopadhyay, "Bennett clocking of nanomagnetic logic using multiferroic single-domain nanomagnets," *Applied Physics Letters*, vol. 97, no. 17, p. 173105, 2010. [Online]. Available: https://doi.org/10.1063/1.3506690

4 M. S. Fashami, K. Roy, J. Atulasimha, and S. Bandyopadhyay, "Magnetization dynamics, bennett clocking and associated energy dissipation in multiferroic logic," *Nanotechnology*, vol. 22, no. 15, p. 155201, mar 2011. [Online]. Available: https://doi.org/10.1088/0957-4484/22/15/155201

5 S. Bandyopadhyay, J. Atulasimha, and A. Barman, "Magnetic straintronics: Manipulating the magnetization of magnetostrictive nanomagnets with strain for energy-efficient applications," *Applied Physics Reviews*, vol. 8, no. 4, p. 041323, 2021. [Online]. Available: https://doi.org/10.1063/5.0062993

6 P. Pathak and D. Mallick, "Straintronic nanomagnetic logic using self-biased dipole coupled elliptical nanomagnets," *IEEE Transactions on Magnetics*, vol. PP, pp. 1–1, 10 2022. [Online]. Available: 10.1109/TMAG.2022.3199589

7 N. D'Souza, M. Salehi Fashami, S. Bandyopadhyay, and J. Atulasimha, "Experimental clocking of nanomagnets with strain for ultralow power boolean logic," *Nano Letters*, vol. 16, no. 2, pp. 1069–1075, 2016, pMID: 26744913. [Online]. Available: https://doi.org/10.1021/acs.nanolett.5b04205

8 J. Liu, X. Yang, M. Zhang, B. Wei, C. Li, D. Dong, and C. Li, "Efficient dipole coupled nanomagnetic logic in stress induced elliptical nanomagnet array," *IEEE Electron Device Letters*, vol. 40, no. 2, pp. 220–223, 2019. [Online]. Available: https://doi.org/110.1109/LED.2018.2889707

9 G. Csaba, A. Imre, G. Bernstein, W. Porod, and V. Metlushko, "Nanocomputing by field-coupled nanomagnets," *IEEE Transactions on Nanotechnology*, vol. 1, no. 4, pp. 209–213, 2002. [Online]. Available: https://www.doi.org/10.1109/TNANO.2002.807380

10 M. Kazemi, E. Ipek, and E. G. Friedman, "Adaptive compact magnetic tunnel junction model," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3883–3891, 2014. [Online]. Available: https://www.doi.org/10.1109/TED.2014.2359627

11 A. Jaiswal, A. Agrawal, and K. Roy, "In-situ, in-memory stateful vector logic operations based on voltage controlled magnetic anisotropy," *Scientific Reports*, vol. 8, no. 1, p. 5738, 2018. [Online]. Available: https://www.doi.org/10.1038/s41598-018-23886-2

12 M. Long, L. Zeng, T. Gao, D. Zhang, X. Qin, Y. Zhang, and W. Zhao, "Self-adaptive write circuit for magnetic tunneling junction memory with voltage-controlled magnetic anisotropy effect," *IEEE Transactions on Nanotechnology*, vol. 17, no. 3, pp. 492–499, 2018. [Online]. Available: https://www.doi.org/10.1109/TNANO.2018.2815721

13 J. Song, I. Ahmed, Z. Zhao, D. Zhang, S. S. Sapatnekar, J.-P. Wang, and C. H. Kim, "Evaluation of operating margin and switching probability of voltage- controlled magnetic anisotropy magnetic tunnel junctions," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 4, no. 2, pp. 76–84, 2018. [Online]. Available: https://www.doi.org/10.1109/JXCDC.2018.2880205

14 M. M. Torunbalci, P. Upadhyaya, S. A. Bhave, and K. Y. Camsari, "Modular compact modeling of mtj devices," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4628–4634, 2018. [Online]. Available: https://www.doi.org/10.1109/TED.2018.2863538

15 T. Gao, L. Zeng, D. Zhang, Y. Zhang, K. L. Wang, and W. Zhao, "Compact model for negative capacitance enhanced spintronics devices," *IEEE Transactions on Electron Devices*, vol. 66, no. 6, pp. 2795–2801, 2019. [Online]. Available: https://www.doi.org/10.1109/TED.2019.2908957

16 S. Verma, R. Paul, and M. Shukla, "Non-volatile latch compatible with static and dynamic cmos for logic in memory applications," *IEEE Transactions on Magnetics*, vol. 58, no. 4, pp. 1–8, 2022. [Online]. Available: https://www.doi.org/10.1109/TMAG.2022.3149811

17 L. Xu, L. Cai, H. Q. Cui, S. Wang, X. K. Yang, and C. W. Feng, "Hspice circuit modeling of the strain-mediated multiferroic heterostructure device," *Micronanoelectronic Technology*, vol. 54, no. 3, pp. 145–149, 2017.

18 M. S. Fashami, K. Munira, S. Bandyopadhyay, A. W. Ghosh, and J. Atulasimha, "Switching of dipole coupled multiferroic nanomagnets in the presence of thermal noise: Reliability of nanomagnetic logic," *IEEE Transactions on Nanotechnology*, vol. 12, no. 6, pp. 1206–1212, 2013. [Online]. Available: https://www.doi.org/10.1109/TNANO.2013.2284777