# Frequency-to-Voltage Converter Based Dual-Loop PLL with Variable Phase Locking Capability

**Z M Saifullah[1], Paul M Furth[1], SriHarsh Pakala[1], and Alejandro Roman-Leora[2]**

[1] *Department of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM, USA*
[2] *Universidad Autonoma de Aguascalientes, Electronic Systems Department, Mexico*

Email: zmsaif@nmsu.edu, pfurth@nmsu.edu, sriharsh.pakala@gmail.com, alejandro.roman@edu.uaa.mx

A novel frequency-to-voltage converter (FVC) based phase-locked loop (PLL) is proposed to overcome the inability of an FVC-based frequency-locked loop (FLL) to lock phase. The proposed dual-loop PLL adds variable phase-locking capability, such that the phase locking angle can vary from 0° – 360°. The additional variable phase-locking can be applied in data communication in the form of phase modulation. The design is targeted for a 0.5-µm CMOS process. The proposed design generates a 480MHz clock from a reference clock of 15MHz. In simulation, the proposed PLL locks within 3.56 µs while consuming 1.61 mW of power.

*Introduction:* The PLL is a widely-used device in modern data communication systems, especially for recovering data from a receiver channel and generating a low-cost high-frequency clock from a low-frequency reference. Since high-speed data transfer can result in missing digital information, it is more important than ever to have an accurate, synchronous, time-domain circuit to retrieve incoming data.

An FVC-based FLL was proposed in [1]. Since FVC-based designs are based on the charging and discharging of capacitors, they are naturally very fast. An FLL generates an output clock signal which has a frequency that is related to that of a reference signal, but with unknown phase. They are commonly used to generate an output clock that is $N$ times higher than the reference clock. As described in [1, 2], an FVC-based FLL can also generate a desired output frequency without any reference clock, using a reference voltage as one of the error amplifier's inputs in the FVC block. However, the FLL comes with an inherent deficiency, which restricts their use in data communication system: the lack of phase control. As such, the phase of the FLL slowly changes with time and, hence, is unsynchronized with the reference clock.

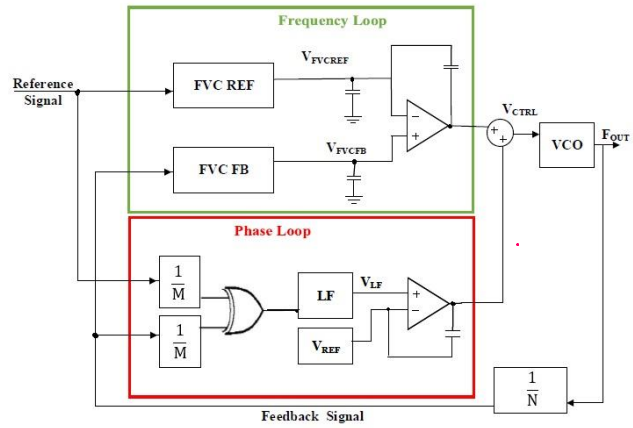


**Fig 1** *Block Diagram of Proposed PLL*

In [3, 4], researchers propose dual-loop PLLs that add FVC-based control to conventional charge-pump-based PLLs. They report improved jitter performance. However, one drawback to the design in [3] is the use of large capacitors (> 250 pF) in the lowpass filter.

Since the FVC-based FLL is very fast, it maintains high-power supply rejection [1]. An FVC-based PLL should have similar supply rejection performance, with added control over phase locking. The objective of this letter is to introduce a low power FVC-based clock-multiplying PLL which locks the phase at any desired angle with respect to the reference signal. The proposed design targets a standard 0.5-µm CMOS process.

*Proposed FVC-based PLL scheme:* A conventional PLL consists of a phase detector (PD), charge pump (CP), low-pass filter (LF) and voltage-controlled oscillator (VCO). The PLL may also include frequency dividers and mixers when used in frequency-synthesizing applications [5, 6]. An FVC-based FLL however, employs a frequency-to-voltage converter and an error amplifier. The FVC can be implemented with a ramp generator and sample-and-hold circuit [1-4].

The block diagram of the proposed FVC-based PLL is shown in Figure 1. The proposed design consists of two control loops. The first loop, the frequency loop, is responsible for frequency locking and frequency multiplication. This loop contains two FVC blocks. Each FVC block consists of a ramp generator with a fixed bias current, and a sample-and-hold circuit, which samples the peak at the end of each cycle. The output voltage from an FVC depends on the capacitor size, bias current and charging time. To ensure 50% duty cycle, the input clock is divided by two. Denoting the input frequency of an FVC as $F_{IN}$, bias current $I$, and charging capacitor $C$, then the output voltage $V_{FVC}$, from the FVC block follows:

$$V_{FVC} = \frac{I}{C} \cdot \frac{1}{F_{IN}}$$

Note that that as $F_{IN}$ increases, $V_{FVC}$ decreases, producing an inherent inversion, such that the overall frequency loop has negative feedback. One FVC block converts the reference frequency to a voltage, the other one converts the feedback signal to a voltage. An operational transconductance amplifier integrator (OTA-C) is used to compare the signals and integrate the error, or difference, between them. When both signals are equal, the generated output from the OTA-C, which drives the VCO, becomes constant and the feedback signal is considered locked at the desired input reference frequency.

The second loop, the phase loop, performs average-based phase locking. This loop consists of a XOR PD, an averaging LF, and an OTA-C. The phase difference between the reference and feedback signals is detected by the XOR gate. The digital output of the XOR PD is averaged through a first-order LF and gets compared at the OTA with reference voltage $V_{REF}$ to achieve the desired phase difference.

Note that the proposed PLL does not require any charge pump. In the proposed scheme, both control loops work with a single feedback signal, in a cooperative manner. The frequency loop is designed to be faster than the phase loop with the help of higher bias current in the OTA-C, so that frequency-locking can be achieved first. Once the frequency is locked, the phase loop ensures the PLL will lock in phase. Error signals from each loop are converted to currents via the OTA-Cs. These currents are summed at the control signal $V_{CTRL}$ at the input of the VCO, which generates the desired output signal.

The linearized model of the proposed PLL is shown in Figure 2. As shown, the proposed design has two control loops which are generated from a single feedback signal after output $F_{OUT}$ is divided by N. The open-loop transfer function of the proposed block is:

$$H(s) = \left\{ (K_{FVCFB} \cdot \frac{1}{N} \cdot \frac{K_{INTF}}{s}) + (\frac{V_{DD}}{\pi . N . M . s} . H_{LF} . \frac{K_{INTP}}{s}) \right\} . K_{VCO}$$

Here, $K_{FVCREF}$, $K_{FVCFB}$, $K_{INTF}$, $K_{VCO}$, $H_{LF}$, $K_{INTP}$, $V_{DD}$, $M$ and $N$ are the gain of the reference FVC, gain of feedback FVC, gain of integrator of frequency loop, gain of VCO, transfer function of LF, gain of integrator of phase loop, supply voltage, divide-by ratio for the PD, and divide-by ratio for the feedback signal, respectively.

Figure 3 shows the simulated magnitude and phase for the proposed PLL along with that of an FVC-based FLL. The FLL has only the frequency-locking loop, whereas the proposed PLL has frequency and phase-locking loops. The FVC-based FLL is an integrator, as shown. In the proposed design, however, frequency and phase loops are summed together. The proposed PLL shows much higher gain at low frequencies than that of the FVC-based FLL. The overall loop bandwidth of the proposed design remains unchanged.

The XOR-based PD detects the phase difference between the reference clock and the feedback signal and converts that difference to a digital output, which is then averaged by a first-order LF. The XOR-based PD has lower complexity, area and power in comparison with a conventional charge-pump-based PD. The output of the LF ($V_{LF}$) is then fed to one input of the OTA-C. The other input of the OTA-C is a control voltage ($V_{REF}$) that represents the desired phase difference between the reference and feedback signals. The OTA-C computes the error between $V_{LF}$ and $V_{REF}$. The error signal adjusts the control signal for the VCO and, via negative feedback, ensures both inputs of the OTA-C are equal.

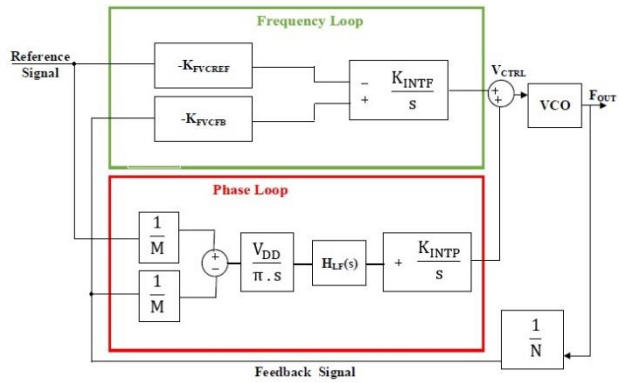


**Fig 2** *Linearized model of proposed design*

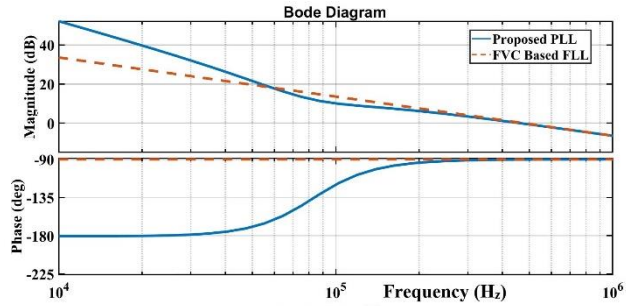


**Fig 3** *Open-loop frequency response for FVC-based FLL and Proposed PLL.*

The average output of the XOR PD after passing through an LF ($V_{LF}$) varies from 0V to $V_{DD}$, where 0V represents 0° phase difference and $V_{DD}$ represent 180° phase shift. The relation is linear between $V_{LF}$ and phase difference. Variations in duty cycle between $F_{IN}$ and $F_{REF}$ are eliminated by dividing both clock inputs by 2. These additional divide-by-two circuits extend the phase range of the XOR PD to 0°-360° where 0V represents 0° phase difference and $V_{DD}$ now represents 360°. Due to the type of input stage (NMOS or PMOS) in the OTA, it is not possible to achieve the full range from 0° to 360°. This limitation can easily be eliminated by further dividing both input signals before sending them to the PD. Signals can be divided by $M = 2^i$ with the addition of $i$ DFFs. The relation of phase difference and $V_{REF}$ becomes:

$$\theta = \frac{V_{REF}}{V_{DD}}.180.M$$

Here, $\boldsymbol{\theta}$, $V_{REF}$, $V_{DD}$ and $M$ are the desired phase difference, reference voltage, supply voltage, and divided value, respectively. For example, if M = 4, $V_{DD}$ = 3.6 V, and $V_{REF}$ = 1.8 V, the proposed PLL will lock at 360°, which is equivalent to 0°. And to achieve the entire +/-180° range, $V_{REF}$ need only vary from 0.9V to 2.7 V. Hence, we no longer need to operate near either supply rail.

As an added feature for this PLL, variable-angle phase locking can be exploited to produce phase modulation by programming a time-varying voltage at node $V_{REF}$.

*Results:* The proposed FVC-based dual-loop PLL was simulated in a 0.5-µm CMOS process. Simulations were performed using Analog Devices's LTspice with a 3.6-V power supply. The FVC current was chosen to be 12 µA with a 1-pF charging capacitor. Total power consumption for a 15 MHz reference input and 480 MHz output was simulated as 1.61 mW. A similar FVC-based FLL, without phase locking, would consume 1.504 mW, that is, only 6.6% less power than the proposed PLL. As such, the power overhead to achieve phase locking is minimal. The proposed PLL has a simulated lock time of 3.56 µs, whereas a similar FLL without phase detection locks in 2.4 µs. Lock time is defined as the time from power-ON to the time at which the PLL locks.

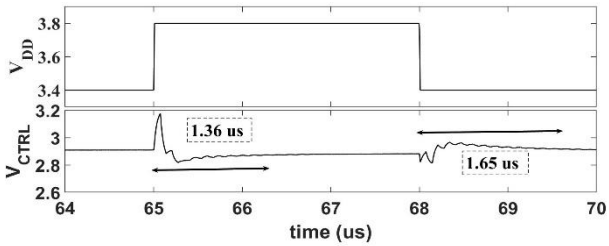


**Fig 4** *Simulated supply-voltage transient response.*

Figure 4 shows a simulated supply voltage transient from 3.4 V to 3.8 V and from 3.8 V to 3.4 V. For the proposed PLL, the recovery times (within 0.1% of $V_{CTRL}$ final value) are 1.36 µs and 1.65 µs, for positive- and negative-going supply transients, respectively. The period of the 15-MHz reference clock is 66.7 ns. As such, the proposed PLL takes less than 25 cycles of the reference clock to recover.

A 50-kHz 1-Vpp sinusoidal signal was added to the 3.6-V power supply of the proposed PLL. The maximum value of the output frequency was found to be 2 MHz above the desired output frequency of 480 MHz and the minimum value was 10 MHz below the desired output frequency, which corresponds to +0.42% and -2.08% variation, respectively.

The proposed PLL can lock the output clock at any phase with respect to the input reference clock. Figure 5 shows a linear relationship between $V_{REF}$ and the phase locking angle, while achieving a full 360° range of locking angle.

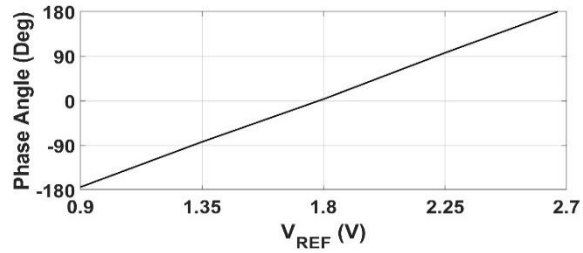


**Fig 5** *Simulated phase-locking angle as a function of $V_{REF}$*

*Table 1. Performance comparison of proposed PLL with prior work*

| Reference Work | [3] | [7] | [8] | **This Work** |
|---|---|---|---|---|
| Input Freq. (MHz) | 37.5 | 14 | 64 | **15** |
| Output Freq. (MHz) | 1500 | 448 | 2400 | **480** |
| Power (mW) | - | 120 | 29.6 | **1.61** |
| Lock Time (µs) | 5 | 18 | 20 | **3.56** |
| Total Capac. (pF) | >250 | >37000 | >2000 | **~45** |

*Conclusion*: As shown in Table 1, the proposed PLL demonstrates lower power consumption, reduced lock time and significantly smaller total capacitance value in comparison to published work in the table.

## References


1. Abdelouahab Djemouai, Mohamad A. Sawanand Mustapha Slamani.: New frequency-locked loop based on CMOS frequency-to-voltage converter: design and implementation, IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing, vol. 48, no. 5, May 2001
2. Sri Harsh Pakala, Punith R. Surkanti, and Paul M. Furth.: A spread-spectrum mode enabled ripple-based buck converter using a clockless frequency control, IEEE Transactions on Circuits and Systems – II: Express Briefs, vol. 66, no, 3, March 2019.
3. Dae Hyun Moon and Young Shig Choi.: Two-negative feedback loop PLL with frequency voltage converter loop, IDEC Journal of Integrated Circuits and Systems, vol 5, no.4, October 2019
4. Xuefan Jin, Kee-Won Kwon, Young-Shig Choi, and Jung-Hoon Chun.: A dual-loop phase locked loop with frequency to voltage converter, Journal of Semiconductor Technology and Science, vol. 19, no.2, June 2019.
5. V. V. Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra.: A 320 MHz, 1.5 mW @ 1.35 V CMOS PLL for microprocessor clock generation, IEEE J. Solid-State Circuits, vol. 31, pp. 1715–1722, Nov. 1996.
6. D. L. Chen.: A power and area efficient CMOS clock/data recovery circuit for high-speed serial interfaces, IEEE J. Solid-State Circuits, vol. 31, pp. 1170–1176, Aug. 1996.
7. Yang, C.-Y., & Liu, S.-I.: Fast-switching frequency synthesizer with a discriminator-aided phase detector. IEEE Journal Solid-State Circuits, vol. 35, pp. 1445–1452, Oct. 2000.
8. Woo, K., Liu, Y., Nam, E., & Ham, D.: Fast-lock hybrid PLL combining fractional-N and integer-N modes of differing bandwidths. IEEE J. Solid-State Circuits, vol. 43, 379–389, Feb. 2008.