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A 2.72 μ s row conversion time 11-bit column parallel single slope ADC with differential-clocks-assisted TDC interpolation for CMOS image sensor

Hao Duan[1], Kaiming Nie[1], and Jiangtao Xu[1]

[1]Tianjin University School of Microelectronics

April 16, 2024

Abstract

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Hao Duan[1,2] | **Kaiming Nie**[1,2] | **Jiangtao Xu**[1,2]

[1]School of Microelectronics, Tianjin University, Tianjin, China

[2]Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, Tianjin, China

Correspondence
Kaiming Nie, School of Microelectronics, Tianjin University,Tianjin, China
Email: nkaiming@tju.edu.cn

Present address
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Abstract

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KEYWORDS
CMOS image sensor, column-parallel ADC, differential-clocks-assisted TDC (DCA-TDC), single-slope (SS) ADC

1 | INTRODUCTION

In recent years, CMOS image sensors (CISs) have been widely used in various fields due to their outstanding advantages of low power consumption and high speed, compared to charge-coupled devices (CCDs)[1]. The current trend in CMOS image sensors is to use larger pixel arrays, achieve faster frame rates, and consume lower power. As the prominent component in image sensors, the A/D converter determines the overall performance of the device. Therefore, the requirements for speed and power of ADCs are being emphasized, particularly in image sensors that capture higher pixel resolution pictures and faster frame rate videos[2].

Nowadays, various types of ADCs used in CISs have been studied, such as successive approximation register (SAR) ADCs[3], cyclic ADCs[4], and single-slope (SS) ADCs[5,6,7,8]. However, the SS ADCs are mainstream and widely used in column parallel ADCs. This structure contains a comparator and a counter, making it simpler than other types of ADCs. It can also be easily implemented with a narrow column pitch. Furthermore, SS ADCs have lower power dissipation than cyclic ADCs and occupy less silicon area than SAR ADCs. At last, the SS ADCs have better column uniformity than other types of ADCs[9].

However, the drawback of SS ADCs is also significant. For N-bit SS ADCs, the quantization time is 2^N main clock periods, resulting in a relatively slow quantization speed (here, N represents the resolution of the ADC). Compared to SS ADCs, the SAR ADCs, and cyclic ADCs require only N main clock periods for one quantization process, respectively. For applications involving CISs with large pixel arrays and high frame rates, the speed of SS ADCs is a critical factor to consider.

One of the structures that accelerates conversion speed is the two-step (TS)-based SS ADCs. The N-bit ADC requires $(2^C + 2^F)$ conversion steps[10,11,12,13,14,15]; where C and F represent the number of coarse bits and fine bits, respectively (N = C + F). The

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multiple-ramp single slope (MRSS) ADC[10], for example, utilizes multiple fine ramp generators for the fine quantization process. However, this approach results in high power consumption and requires a large silicon area. The modified structure based on MRSS is TS SS ADC, which utilizes holding capacitors as an analog memory to sample the coarse steps. Although this scheme involves only two ramp generators, the main challenge in design is the issue of linearity caused by the use of multiple ramp slopes[11]. Using a first-step half-reference ramping (FHR) scheme avoids the aforementioned problems[12]. However, the use of the binary-weighted search algorithm can only retrieve the most significant bit (MSB) information, while the remaining lower bits still require a significant amount of time, especially as the resolution of the SS ADC increases. The FHR scheme needs to correct the error at the center voltage of the quantization range and necessitates error calibration.

Another approach involves converting fine quantization steps into the time domain, utilizing the improved temporal resolution provided by nanometer-scale devices[16]. A SS ADC with the MSB priority quantization based on cyclic TDC is proposed[17]. This structure can shorten the search range of the ramp by almost half. However, the cyclic TDC interpolation circuit increases power consumption. The TDC can also be achieved through a set of multi-phase clock signals that can capture the phase information. Generally, interpolating an N-bit flash time-to-digital converter (FTDC) can improve the conversion speed by a factor of 2^N. And to ensure precise phase delay in column FTDCs, it is necessary to balance the variations in PVT (process, voltage, temperature) by using a delay-locked loop (DLL). In their study[18], the authors propose the utilization of open-loop, local per-128 column delay lines with FTDC code redundancy as a means to mitigate challenges associated with DLL design and clock generation. However, including a calibration circuit is essential to accommodate variations in PVT, thereby increasing system complexity.

In this study, we propose a SS ADC with differential-clocks-assisted time-to-digital converter (DCA-TDC) interpolation for high frame-rate CISs. The N-bit ADC is divided into (C+F)-bit, where C and F represent the number of coarse bits and fine bits, respectively. On the one hand, the utilization of the DCA-TDC structure shortens the quantization range in the time domain by a factor of 2^F compared to a traditional SS ADC. On the other hand, by employing a binary-weighted search algorithm to determine the MSB (i.e., the F-bit) of fine quantization, the search range for fine quantization is limited to half a period of the main clock. In this way, the DCA-TDC only utilizes 2^{F-1} delay chain units, which are only half the number of ordinary TDC delay chain units, to resolve the least significant (F-1)-bit. The optimized DCA-TDC delay chain reduces the layout area, dynamic power, and conversion time from thermometer to binary codes introduced by half compared to an ordinary TDC delay chain.

The article is organized as follows: Section II describes the overall architecture of the proposed ADC. Section III provides an overview of the circuit implementation details. Section IV presents the significant simulation results of this study. Section V provides the concluding remarks.

2 | PROPOSED READOUT SCHEME

2.1 | Conventional SS ADC

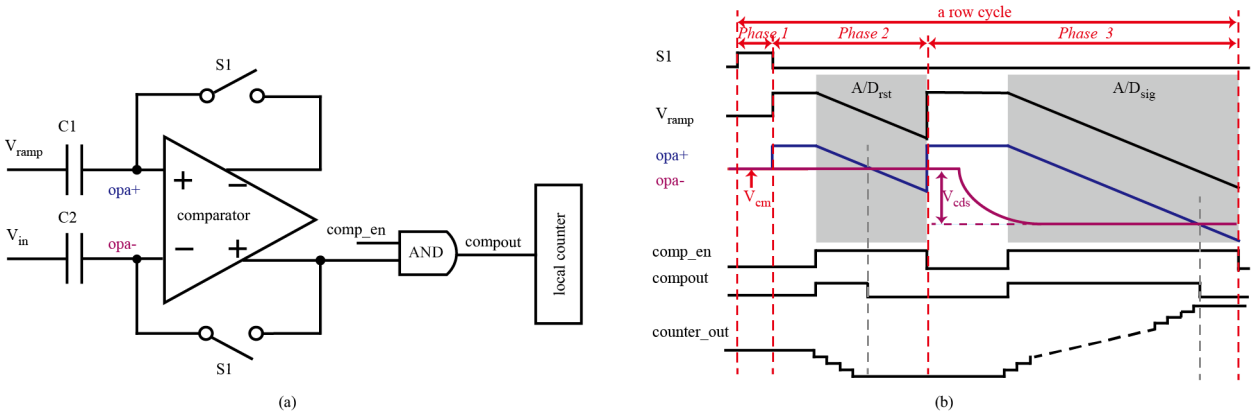

FIGURE 1 (a) Simplified conventional column-parallel SS ADC and (b) its operational timing diagram and waveform.

Fig. 1(a) shows a conventional column-parallel SS ADC. Each column is composed of a comparator with two sampling capacitors (C1 and C2), switches (S1s), an N-bit counter, and a shared ramp generator that is utilized by all column SS ADCs. Each column's SS ADC is ac-coupled by a reference signal (V_{ramp}) derived from the ramp generator, as well as an input signal (V_{in}) obtained from the pixel. The operational timing diagram and waveform of the traditional SS ADC with digital correlated double sampling (D-CDS) are shown in Fig. 1(b). D-CDS, which is performed in the digital domain, is widely used due to its high noise suppression capability [12]. At the beginning of each row cycle, the photodiode is reset and the pixel signal is V_{rst}. After exposure, the pixel signal becomes V_{sig}.

During Phase 1, when S1 turns on, both the *opa+* and *opa–* maintain the same voltage level, which is denoted as V_{cm}. The capacitors C1 and C2, with the same capacitance, sample the voltage differences $V_{cm} - V_{ramp}$ and $V_{cm} - V_{rst}$, respectively. During Phase 2, when the control enable signal of *comp_en* is triggered, the comparator starts comparing the *opa+* and *opa–* while the V_{ramp} decreases simultaneously. In the A/D_{rst} period, if the *opa–* signal exceeds the *opa+* signal, the output of the comparator (*compout*) changes, the counter ceases counting in subtractive mode, and the results of the A/D_{rst} is obtained. During Phase 3, the pixel signal changes from V_{rst} to V_{sig}, and a value of $V_{cm} - V_{cds}$ is generated at the *opa–*, where the $V_{cds} = V_{rst} - V_{sig}$, and represents the photodiode voltage. The A/D_{sig} period is similar to the A/D_{rst} period, while the counter operates in additive mode and counts based on the results of the A/D_{rst}. Finally, the digital codes in the counter represent the photodiode voltage. In this way, the offset error and noise are further suppressed.

However, it should be noted that an N-bit SS ADC needs at least 2^N counter clocks during the A/D_{sig} ramp searching period. When the bit-depth of SS ADC increases, the conversion time also increases exponentially. To enhance the conversion speed of the SS ADC combined with D-CDS, the study adopts DCA-TDC interpolation method in the digital domain. Since the ordinary counter has a wide dynamic quantization range and low temporal resolution, and the TDC has a narrow quantization range and high temporal resolution [19], the DCA-TDC interpolation combines these two time digitizers to reduce the conversion time. For a (C+F)-bit SS ADC, the ramp searching period is reduced to 2^C clock cycles and the least significant F-bit can be resolved by DCA-TDC.

2.2 | Operational Principle of Proposed SS ADC

2.2.1 | Combination Method between the Coarse and Fine Quantization

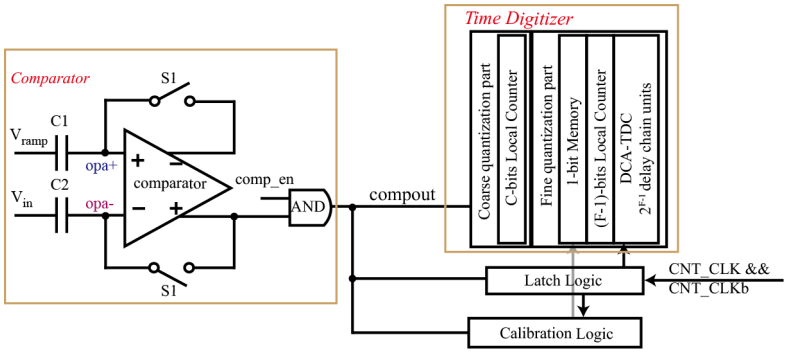

FIGURE 2 Simplified schematic diagram of the proposed SS ADC.

Fig. 2 presents a simplified schematic diagram of the proposed SS ADC. The system is comprised of one comparator, time digitizer, and digital logic, including latch logic and calibration logic. The comparator has the same structure as the ones in conventional SS ADC. The time digitizer consists of a coarse and fine quantization part. The coarse quantization part is composed of a C-bit local counter. The fine quantization part is composed of a 1-bit memory for the F-bit, an (F-1)-bit local counter, and a DCA-TDC delay chain.

To provide a clear explanation of the proposed scheme, the working waveform of the proposed SS ADC is shown in Fig. 3. The entire row cycle is implemented in four phases.

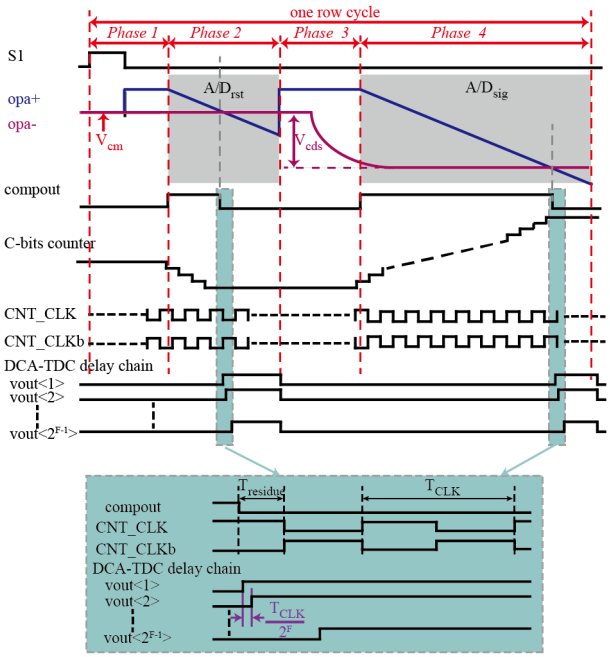

FIGURE 3 The operational waveform of the proposed SS ADC.

During Phase 1, S1s turn on and the comparator is in a reset state. The ramp signal, V_{ramp}, and the pixel reset signal, V_{rst}, are sampled by capacitors C1 and C2, respectively.

During Phase 2, the V_{ramp} exhibits a gradual decrease with a consistent slope. The *CNT_CLK* drives the C-bit local counter to quantize the time interval, which begins from the start of Phase2 to the moment the *compout* signal changes. The coarse quantization results are stored in C-bit local counter. When the *compout* changes, the binary-weighted search algorithm helps recognize whether *CNT_CLK* is low or *CNT_CLK* is high when the *compout* changes, and the 1-bit memory stores this information as the MSB (i.e., the F-bit) of the fine quantization immediately. At the same time, the DCA-TDC delay chain units are stimulated to measure the time residue $T_{residue}$ with high temporal resolution.

It is worth noting that the $T_{residue}$ starts from the moment the *compout* changes and ends at the following rising edge of either *CNT_CLK* or *CNT_CLKb*. If the F-bit is low, the following rising edge of *CNT_CLK* ends the quantization of DCA-TDC. If the F-bit is high, the following rising edge of *CNT_CLKb* ends the quantization of DCA-TDC. By this way, the search range for fine quantization is limited to half a period of the main clock T_{CLK}. The DCA-TDC only requires 2^{F-1} delay chain units, which is only half the number of delay chain units needed by ordinary TDC, in order to resolve the least significant (F-1)-bit. The specific operation of fine quantization is explained in the next section.

The code of the quantization result after the A/D_{rst} is

$$D_{rst} = D_{rst\_C} + M_{em\_rst} + D_{rst\_F-1} \tag{1}$$

where the D_{rst_C} represents the C-bit counter codes of the coarse quantization part, M_{em_rst} represents the 1-bit memory result (i.e., the F-bit), and D_{rst_F-1} represents the (F-1)-bit in the form of thermometer codes that are stored in a DCA-TDC delay chain.

During Phase 3, the pixel signal changes from V_{rst} to V_{sig}, and the (V_{sig} - V_{rst}) is coupled to the *opa+* node. The (F-1)-bit in the form of thermometer codes are converted to binary codes through a logic-shift operation, and the time wasted on the conversion process can be reduced by half. This process can be referred to in Section 3.2 for a clear explanation.

During Phase 4, the quantization process is similar to Phase 2. The code of the quantization result following the A/D_{sig} is

$$D_{sig} = D_{sig\_C} + M_{em\_sig} + D_{sig\_F-1} \tag{2}$$

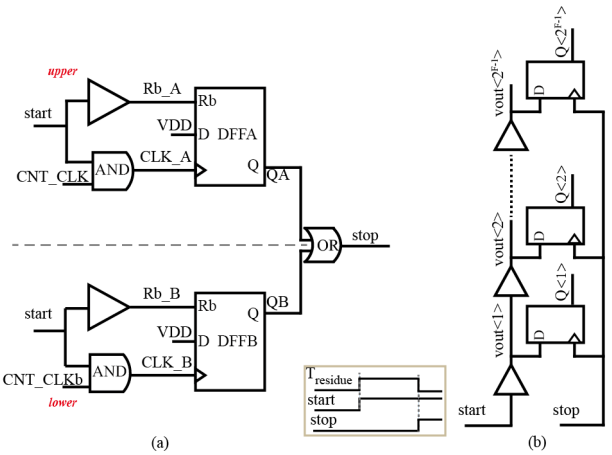

FIGURE 4 (a) Latch Logic circuit and (b) DCA-TDC delay chain.

where the D_{sig_C} represents the C-bit counter codes of the coarse quantization part, M_{em_sig} represents the 1-bit memory result (i.e., the F-bit), and D_{sig_F-1} represents the (F-1)-bit in the form of thermometer codes that are stored in a DCA-TDC delay chain.

The SS ADC operates in pipeline mode. The conversion from thermometer codes to binary codes of the (F-1)-bit occurs in Phase 1 of the following row cycle. By subtracting these two quantization results, the final quantization result is obtained as

$$D_{out} = D_{sig} - D_{rst} \tag{3}$$

To ensure a proper combination of coarse and fine quantization, the temporal resolution of both should be matched. Since the 2^{F-1} delay chain units in DCA-TDC quantize half the period of T_{CLK}, the temporal resolution of the DCA-TDC delay chain units is set

$$\frac{T_{CLK}/2}{2^{F-1}} = \frac{T_{CLK}}{2^F} \tag{4}$$

The proposed SS ADC structure exhibits two distinct differences compared to conventional SS ADCs. Firstly, the implementation utilizes a DCA-TDC interpolation structure to effectively improve the speed of ramp searching by a factor of 2^F. The high C-bit can be generated by a C-bit counter, which covers the full temporal range for quantization with low temporal resolution (T_{CLK}). The low F-bit can be generated by a 1-bit memory and (F-1)-bit DCA-TDC, which covers half of T_{CLK} with high temporal resolution ($T_{CLK}/2^F$). Secondly, it employs a pair of differential clocks (*CNT_CLK* and *CNT_CLKb*) and a binary-weighted search algorithm for the latch logic circuit to reduce the number of DCA-TDC delay units by half, which minimizes the layout area and dynamic power consumption.

2.2.2 | Operational Principle of Fine Quantization

As mentioned above, the total bits of the SS ADC are divided into C-bit for coarse quantization, 1-bit for the memory, and (F-1)-bit for fine quantization. This section explains the operational principle of fine quantization.

The latch logic circuit and DCA-TDC delay chain are related to the process of fine quantization and are depicted in Fig. 4 (a) and (b), respectively. The latch logic circuit utilizes a symmetrical structure and is composed of two DFFs (DFFA and DFFB), two AND gates, two delay gates, and an OR gate. The DCA-TDC delay chain is composed of 2^{F-1} delay units. The *start* signal is the *compoutb* signal, which is the inverse of *compout*. It is responsible for triggering DCA-TDC delay chain and enabling the operation of DFFA and DFFB during the fine quantization. The *stop* signal, generated by performing the OR logic operation through *QA* and *QB*, is used to terminate fine quantization by latching vout<1: 2^{F-1}> in the DCA-TDC delay chain. The time interval of $T_{residue}$ is equivalent to the duration between the rising edge of the *start* signal to the rising edge of the *stop* signal.

According to the binary-weighted searching algorithm mentioned above, there are two cases, as depicted in Fig. 5 (a) and Fig. 5 (b) respectively.

In Fig. 5 (a), the *start* signal flips at the first half period of *CNT_CLK*, indicating that the *start* signal changes when *CNT_CLK* is low. The rising edge of *CNT_CLK* that follows the *start* flipping drives DFFA to latch VDD, and then causes *QA* to flip from low to high. Since the duration from the rising edge of *start* to the rising edge of *CNT_CLKb* that follows the *start* flipping exceeds half of the period of the *CNT_CLK*, *QB* flips from low to high later than *QA*. The DFFA has priority over DFFB, and signal *QA* dominates the flipping of *stop* signal, which terminates fine quantization and generates the thermometer codes Q<1: 2^{F-1}>.

Similarly, in Fig. 5 (b), the *start* signal flips at the second half period of *CNT_CLK*, indicating that the *start* signal changes when *CNT_CLK* is high. The rising edge of *CNT_CLKb* that follows the *start* flipping drives DFFB to latch VDD, and then causes *QB* to flip from low to high. The DFFB has priority over DFFA, and signal *QB* dominates the flipping of *stop* signal.

The Fig. 5 (c) shows the operational principle of the DCA-TDC delay chain. After the arrival of the *start* signal, the DCA-TDC delay chain is triggered, and the delay units are sequentially triggered as time passes. The temporal interval between the neighboring signals is $T_{CLK}/2^F$, which provides a high temporal resolution. The number of DCA-TDC delay chain units is 2^{F-1}, and the temporal range of the delay chain is half a period of the main clock T_{CLK}. When the *stop* signal arrives, the temporal information of Tresidue is generated as thermometer codes Q<1: 2^{F-1}>.

In both Fig. 5(a) and Fig. 5(b), the DCA-TDC measures the time interval of Tresidue. This implies that the search range for fine quantization is limited to half of T_{CLK}. Thus, the DCA-TDC only needs 2^{F-1} delay chain units, which is only half the number of ordinary TDC delay chain units.

2.2.3 | Calibration Technique

It is noteworthy that there is a delay gate in front of the Rb terminal of DFFA and DFFB. This is to ensure that the *start* signal does not trigger the DFFA or DFFB while the *CNT_CLK* or *CNT_CLKb* is in logic $''1''$, as depicted in Fig. 4 (a). However, if the *start* signal is in close proximity to the rising edge of the *CNT_CLK* (*CNT_CLKb*), it is possible that the DFFA (DFFB) may still be in the reset state. Consequently, this will result in incorrect thermometer codes being generated by the DCA-TDC delay chain units. This section explains the operational technique of calibration.

The calibration logic circuit is depicted in Fig. 6. It is a symmetrical structure consisting of two DFFs, two AND gates, and an OR gate. The signals *QA* and *QB* are generated from the latch logic circuit, as shown in Fig. 4 (a). The D_{out}<F>b connects to the upper AND gate, while the D_{out}<F> connects to the lower AND gate. *QA* samples *QB* in the upper DFF, while *QB* samples *QA* in the lower DFF. The *flag* signal is generated after the OR logic operation.

Two calibration cases are illustrated in Fig. 7 (a) and Fig. 7 (b), respectively.

In Fig. 7 (a), the *start* signal flips at the first half period of *CNT_CLK*, but it is in close proximity to the rising edge of *CNT_CLK*. The first rising edge of *CLK_A* that follows the flipping of *start*, cannot trigger the DFFA because the *Rb_A* signal is still low. The DFFA, *CLK_A*, and *Rb_A* are referred to in Fig. 4 (a). Thus, the second rising edge of *CLK_A* following the flipping of *start* can trigger DFFA. The DFFB experiences the same situation. The second rising edge of *CNT_CLKb* following the flipping of *start* generates the *stop* signal and terminates the fine quantization. The Tresidue should be almost zero. However, the DCA-TDC delay chain units measure the time interval as Δt, which is equal to ($T_{residue} + T_{CLK}/2$). And D_{out}<F:1> is $''1000\cdots000''$ with carry from D_{out}<F:1> to D_{out}<F> occurred. Thus, the DCA-TDC delay chain records incorrect information with a deviation of 2^{N-1} codes from the correct result. By utilizing the upper section of circuits in Fig. 6, the *flag* signal is $''1''$ after the fine quantization. According to the *flag* signal, the ADC data can be modified by 2^{N-1} codes through subtracting $''1000\cdots000''$ from the counter. The entire arithmetic logic is illustrated in Fig. 7 (c).

Similarly, in cases where the *start* signal flips at the second half period of *CNT_CLK*, but the signal is in close proximity to the rising edge of *CNT_CLKb*, as depicted in Fig. 7 (b), the DCA-TDC delay chain generates inaccurate data. By utilizing the lower section of circuits in Fig. 6, the *flag* signal is $''1''$ after the fine quantization. According to the *flag* signal, the ADC data can be modified 2^{N-1} codes by subtracting $''1000\cdots000''$ from the counter. The entire arithmetic logic is illustrated in Fig. 7 (d).

In summary, the *flag* signal generated by the calibration checking circuit can be used to determine whether the calibration process is required for the ADC output. Calibration operations should only be executed when the *flag* signal is set to $''1''$.

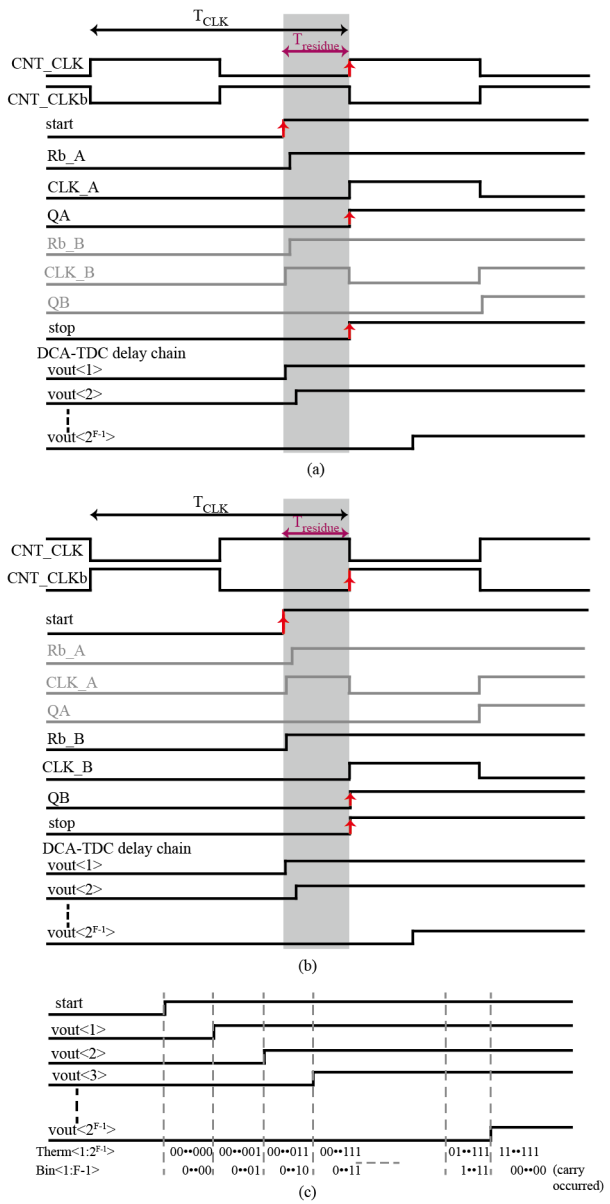

FIGURE 5 (a) The *compoutb* flips at the first half period of *CNT_CLK*, (b) The *compoutb* flips at the second half period of *CNT_CLK*, and (c) Thermometer codes and Binary codes.

3 | CIRCUIT IMPLEMENTATIONS

3.1 | Comparator

A two-stage comparator structure has been chosen to achieve a high gain, as depicted in Fig. 8. This structure incorporates an auto-zeroing (AZ) technique for storing the offset voltage. At the initial state of the comparator, both S1 and S2 are turned on simultaneously. After sampling the input signal, the S1 and S2 switches are sequentially turned off to mitigate the effects of charge injection.

The structures of OPA1 and OPA2 are the same. The hysteresis structure is formed by connecting between the outputs V_{out+} and V_{out-} through M3∼M6, can effectively enhance gain and mitigate the output error induced by noise. The current source, referred to as M7∼M8, employs a cascode configuration to achieve a high output impedance. Given that the primary source

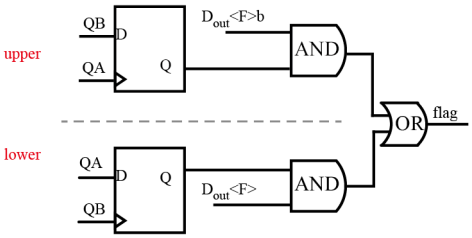

FIGURE 6 Calibration Logic circuit.

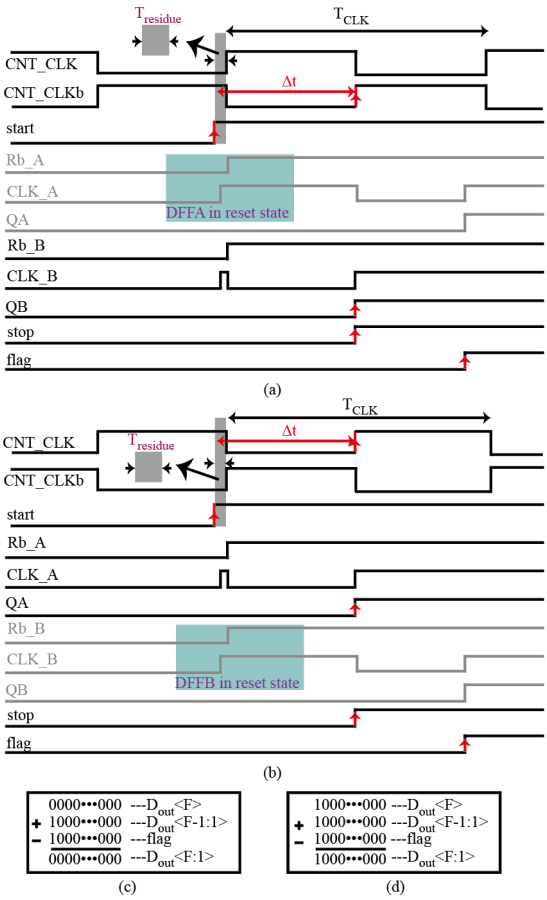

FIGURE 7 (a) The compoutb flips at the first half period of *CNT_CLK*, (b) The compoutb flips at the second half period of *CNT_CLK*, (c) calibration corresponding to (a), and (d) calibration corresponding to (b).

of noise in the system is attributed to the first-stage comparator, OPA1, a larger bias current is allocated to OPA1 compared to OPA2. The 3dB bandwidth of the OPA2 is increased in order to reduce the time delay of the comparator. The performance parameters of OPA1 and OPA2 are presented in Table 1.

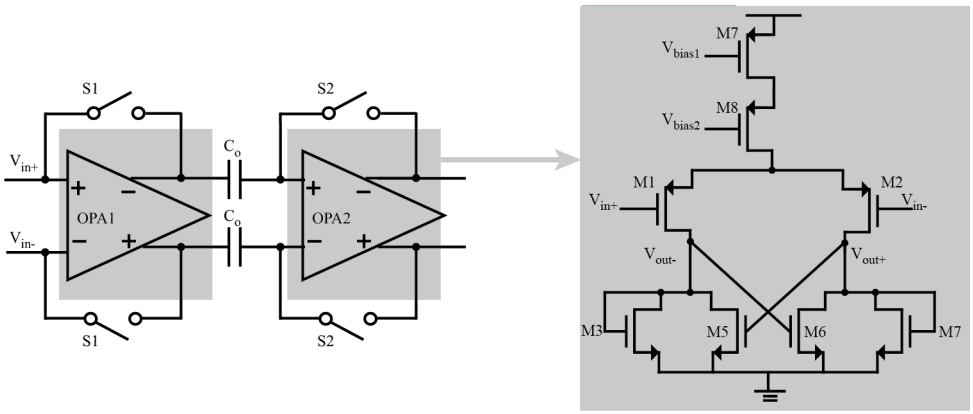

FIGURE 8 The structure of the comparator.

TABLE 1 Parameters of OPA1 and OPA2.

	Current	3dB Bandwidth	Gain
OPA1	5.39μ A	239.8 KHz	42.93 dB
OPA2	2.72μ A	1.357 MHz	43.41 dB

3.2 | Time Digitizer

The time digitizer consists of two parts: a coarse quantization part and a fine quantization part, both of which are located in one column SS ADC. These circuits can achieve the conversion between the additive and subtractive counting algorithms and transition between a holding state and a counting state by utilizing multiplexers. For a comprehensive explanation, the operational procedure that processes the V_{sig} is illustrated in Fig. 9. The circuit is placed in a counting state directly in order to simplify the process. The process of quantizing V_{rst} is similar and will not be elaborated upon in this context.

In this paper, the 11-bit SS ADC is designed with C=6 and F=5.

In Fig. 9 (a), before the *start* signal flips, the main clock *CNT_CLK* drives the LSB of the 6-bit counter in the coarse quantization part, which uses the additive counting algorithm. The *CNT_CLK* operates at a frequency of 62.5 MHz. The 6-bit counter generates the D_{out}<11:6>. After the *start* signal flips, the coarse quantization is interrupted, and the fine quantization commences. The D_{out}<5> is stored in a 1-bit memory by the D<5>. In the meanwhile, the *start* signal activates the DCA-TDC delay chain. To ensure proper synchronization between the coarse quantization and the fine quantization, a temporal resolution ratio of 32:1 (16 ns : 0.5 ns) is implemented. According to the DCA-TDC technique, the fine quantization is terminated by the subsequent rising edge of either *CNT_CLK* or *CNT_CLKb*. This leads to the storage of the fine quantization data in the form of thermometer codes (Q<1:16>). Additionally, it is imperative to provide a global DLL for the DCA-TDC delay chain units in order to compensate for variations in PVT.

In Fig. 9 (b), the decoding stage is presented. The 16 DFFs that belong to the DCA-TDC delay chain are interconnected sequentially between the Q-terminal and D-terminal. The D-terminal of the leftmost one is connected to the ground. As a result, the DCA-TDC delay chain functions as logic-shift circuits. Sequential logic circuits can eliminate the need for additional circuits to decode thermometer codes into binary codes, as compared to combinational logic circuits. The Q-terminal of the rightmost DFF is connected to the input of an AND gate with the signals *CNT_CLKb* and *logic_shift_en*, which is set to "1" during the decoding stage. The ANDOUT signal is connected to the CLK-terminal of D<1>, and the 4-bit counter counts the number of high levels of Q<1:16> in the subtractive counting algorithm. Besides, the D<11:5> are also connected. The outputs of 16 DFFs belonging to the DCA-TDC delay chain are sequentially transmitted by the rightmost DFF. After the decoding stage, the thermometer codes are decoded into binary codes (D_{out}<4:1>). The D_{out}<4:1> is then directly combined with the D_{out}<11:5>, resulting in the generation of D_{out}<11:1>. The time wasted on the decoding stage is reduced by half compared to an ordinary TDC delay chain because the number of DCA-TDC delay chain units is also reduced by half. Specifically, the decoding stage has a duration of $16 \times T_{CLK}$, while it requires $32 \times T_{CLK}$ using the ordinary TDC delay chain.

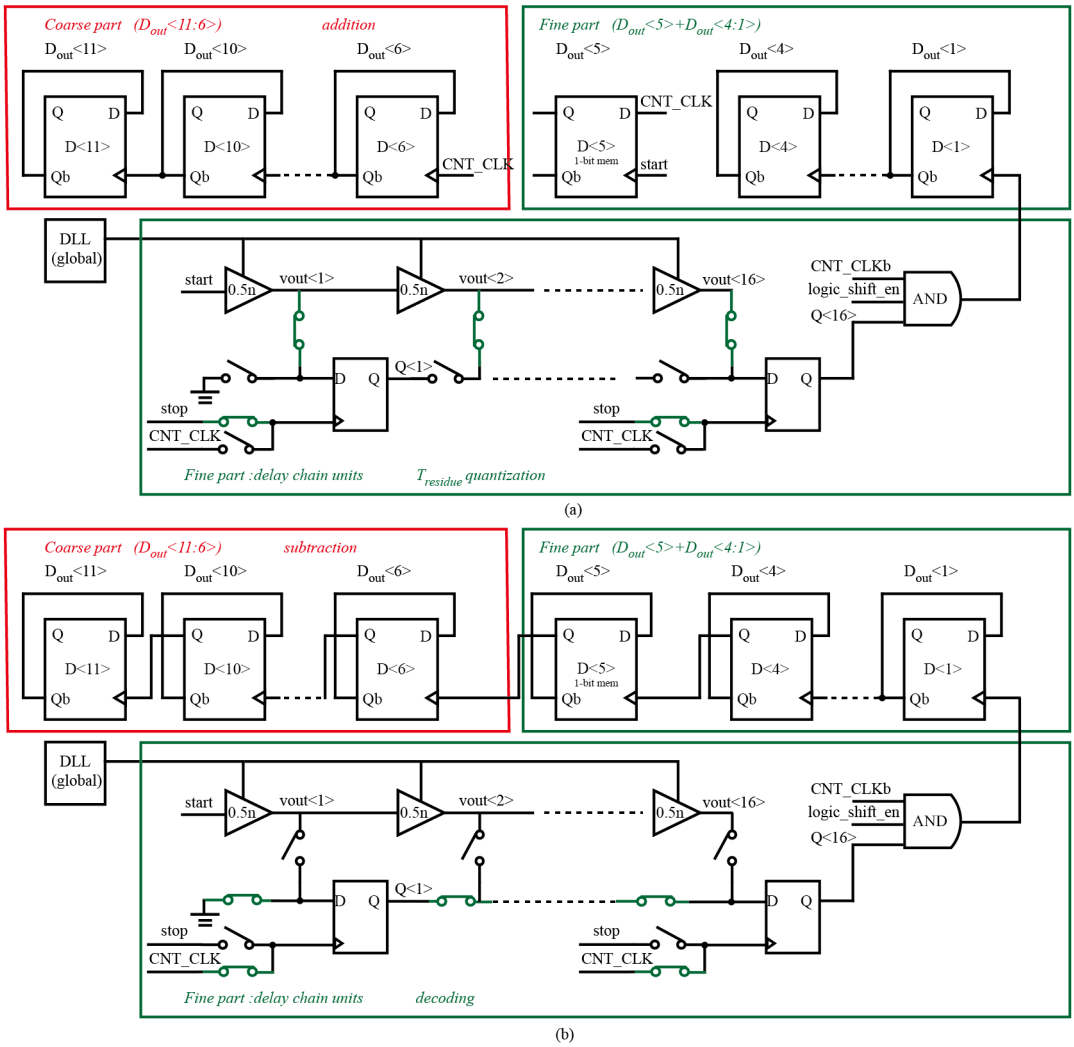

FIGURE 9 (a) Coarse quantization stage/Fine quantization data recording stage and (b) Decoding stage.

4 | SIMULATION RESULTS

In this paper, an 11-bit SS ADC with DCA-TDC interpolation is presented. The circuits were designed and simulated using a standard 0.11μm CMOS process. The main clock operates at a frequency of 62.5 MHz. In this section, the simulation results are obtained through post-simulation analysis. Fig. 10 shows the layout of the proposed 11-bit SS ADC with an area of 6μm$\times$ 1081μm.

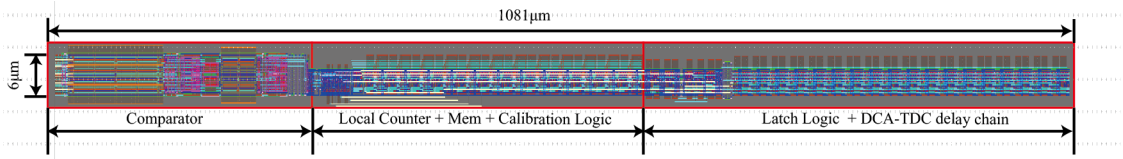

FIGURE 10 The layout of the proposed SS ADC.

A Fast Fourier Transform (FFT) frequency spectrum analysis is performed to examine the dynamic performance of the proposed SS ADC, as shown in Fig. 11. The input sinusoidal signal's frequency is 2.154 KHz, and 512 points are sampled. The simulation results show that the circuits without the calibration technique exhibit worse performance compared to the circuits with the calibration technique. The Signal-to-Noise and Distortion Ratio (SNDR) is 66.47 dB, and the effective number of bits (ENOB) is 10.75 bits for the circuits using calibration technique. In contrast, the SNDR is 48.86 dB, and the ENOB is 7.83 bits for the circuits without calibration technique. This demonstrates the significance and effectiveness of the calibration technique discussed in Section 2.2.3.

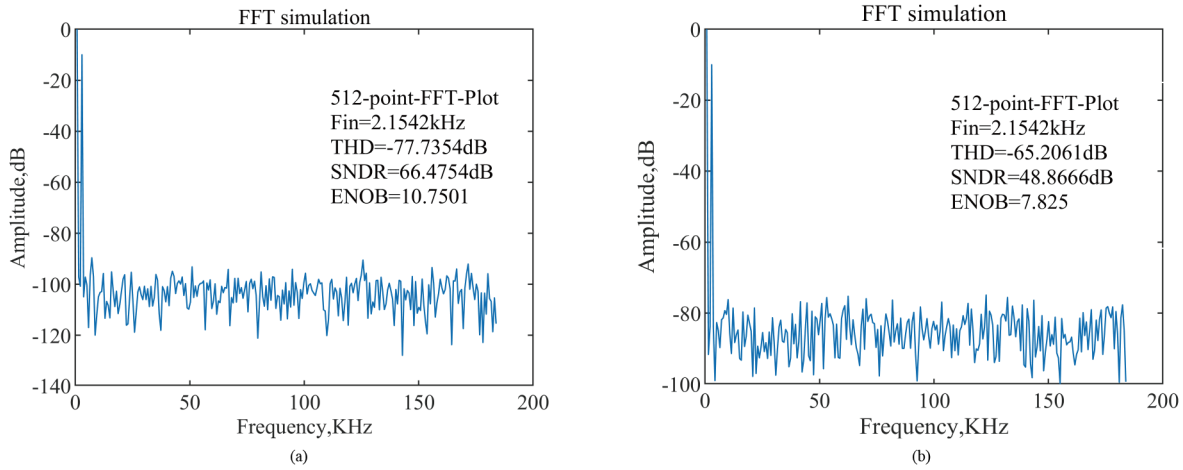

FIGURE 11 The FFT analysis of the SS ADC (a) with and (b) without calibration technique.

Monte Carlo simulation is performed as shown in Fig. 12. The input signal voltage is equal to half of the full range, and 500 points are sampled. The simulation results show that the proposed SS ADC has an average digital code of 1023.67 DN and a standard deviation of 0.50756 DN. This shows that the transistor mismatches in the proposed SS ADC are small enough to maintain uniformity among the SS ADCs in different columns and different chips.

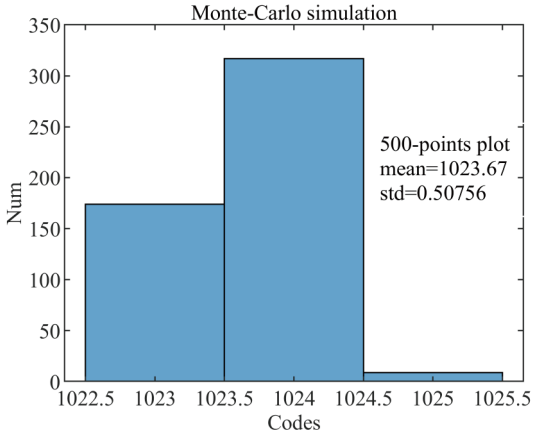

FIGURE 12 Transistor mismatch Monte-Carlo simulations of the SS ADC.

The ENOBs of the proposed SS ADC with PVT changes are presented in Fig. 13. The specific PVT changes include different process corners (ss, tt, ff, sf, fs), voltage supplies (1.35/2.97, 1.5/3.3, 1.65/3.63), and three temperature types (-40°C, 27°C, 80°C). VH, VN, and VL in Fig. 14 represent 1.65/3.63, 1.5/3.3, and 1.35/2.97 voltage supplies, respectively. A total of 45 cases

were simulated. The ENOBs of the proposed SS ADC are mainly distributed around 10.277 bits, with a standard deviation of 0.223 bits. This shows that the proposed SS ADC can achieve significant performance in various PVT environments.

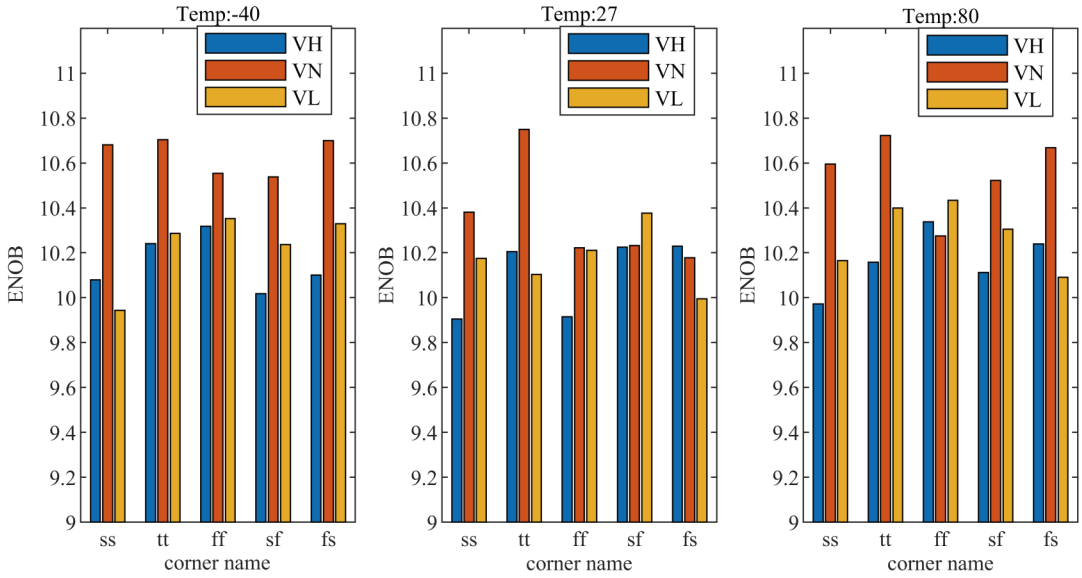

FIGURE 13 ENOBs of the proposed SS ADC with PVT changing.

The power simulation is performed as shown in Fig. 14. The analog supply voltage is 3.3V, and the digital supply voltage is 1.5V in the SS ADC. The power consumption at the column level is 65.4 μW, which includes the shared DLL divided by the number of a group of column SS ADCs. A detailed breakdown of power consumption is shown below.

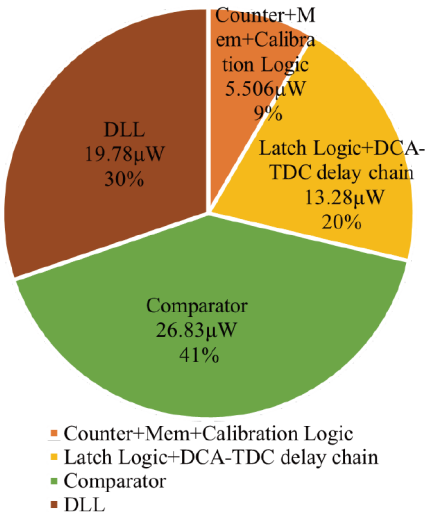

FIGURE 14 Measured division of the power consumption.

Table 2 summarizes the performance comparison between the proposed SS ADC and other reported SS ADCs. The time required for readout of one row cycle is 2.72 μs. Average power consumption is calculated to balance the dynamic power consumption of the counter with inputs at different levels. The Figure of Merit (FoM) is 103.3 fJ/step. Compared to the TS-SS

and other types of SS ADCs with TDC interpolation, the SS ADC with DCA-TDC interpolation introduced in this paper achieves a lower FoM.

TABLE 2 Performance Comparison.

	[20]	[14]	[15]	[6]	[21]	[17]	**This work**[b]
	TCAS-I'20	TCAS-I'20	Sensors	TCAS-I'20	VLSI'22	MJ'23	
	(Meas.)	(Meas.)	(Meas.)	(Meas.)	(Meas.)	(Sim.)	(Sim.)
Process	130nm	110nm	90nm	110nm	130nm	110nm	110nm
Supply (V)	3.3V/1.2V	3.3V/1.5V	2.8V/1.5V	3.3V/1.5V	3.3V/1.2V	3.3V/1.5V	3.3V/1.5V
Structure	SAR	TS-SS	TS-SS	SS	TS-SS	TDC-Interpolated SS	TDC-Interpolated SS
Resolution (bit)	14	8	12	10	12	12	11
ConversionTime (μs)	5	34.72	39.7	34.25	10	2	2.72
ENOB (bit)	11.65	7.45	9.13[c]	8.8	9.8	10.67	10.75
Power (μW)	57	2.4	6.35	56	62	187	65.4
FoM[a] (fJ/step)	89	476	450	4303	696	229.5	103.3

[a]FoM = (Power $\times$ Conversion time)/2^N, where N is the effective number of bits of ADC.
[b]Simulation results in this work.
[c]ENOB is calculated as $log_2(2^b/\varepsilon)$, where 2^b is the ADC output range and ε is the maximum between the worst-case DNL and the input-referred rms noise. This method is the same as [21]'s.

5 | CONCLUSIONS

This paper presents an 11-bit column-parallel SS ADC with DCA-TDC interpolation. The coarse conversion and fine conversion number are 6-bit and 5-bit, respectively. By combining the ordinary counter with a wide dynamic quantization range and low temporal resolution, and the DCA-TDC with a narrow quantization range and high temporal resolution, the quantization range in the time domain is reduced by a factor of 2^5 compared to a traditional SS ADC. The number of DCA-TDC delay chain units is reduced by half with the binary-weighted search algorithm in the temporal domain. The layout area and dynamic power introduced by the DCA-TDC delay chain are reduced by half compared to ordinary TDC delay chain. Besides, the time positions where the *compoutb* flipping occurs are classified into only two cases: the first half period of *CNT_CLK* and the second half period of *CNT_CLK*. This classification enables the application of calibration technique for nonlinearities more easily and effectively than other SS ADCs with TDC interpolation. With a sampling frequency fs of 367.65 KS/s, the ADC achieves THD/SNDR/ENOB of -77.74 dB, 66.47 dB, and 10.75 bits under the 2.154 KHz input signal. The FoM of the SS ADC is 103.3 fJ/step. The simulation results demonstrate that the proposed SS ADC with DCA-TDC interpolation is an effective technique for improving the conversion speed and achieving high performance CISs.

AUTHOR CONTRIBUTIONS

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FINANCIAL DISCLOSURE

None reported.

CONFLICT OF INTEREST

The authors declare no potential conflict of interests.

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