Temperature dependence of ESD effects on 28nm FD-SOI MOSFETs

yiping Xiao[1], Chaoming Liu[1], Yanqing Zhang[1], Chunhua Qi[1], Guoliang Ma[1], Tianqi Wang[1], and Mingxue Huo[1]

[1]Harbin Institute of Technology

April 6, 2023

Abstract

The failure mechanisms caused by electrostatic discharge (ESD) effects at ambient temperatures ranging from -75 to 125 are investigated by Silvaco TCAD simulator. The devices are NMOS transistors fabricated with 28nm fully depleted silicon-on-insulator (FDSOI) technology. Results indicate that with an increase in temperature, the first breakdown voltage of the device decreased by 27.32%, while the holding voltage decreased by approximately 8.49%. The total current density, lattice temperature, and potential etc. were extracted for a detailed insight into the failure process. These findings provide valuable references for the design and development of ESD protection devices applied at different temperature ranges.

Hosted file

`Temperature dependence of ESD effects on 28nm FD-SOI MOSFETs.docx` available at https://authorea.com/users/603873/articles/634011-temperature-dependence-of-esd-effects-on-28nm-fd-soi-mosfets