120 GHz 2-bit reflection-type phase shifter based on PIN diodes switched-lines.

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March 2, 2023

Abstract

In this paper, a 2-bit digital reflection-type phase shifter working at 120 GHz is presented. It uses a compact coupled-lines coupler with low insertion loss and high isolation over a wide bandwidth. The loads are made by a microstrip-line loaded by three PIN diodes whose states are tuned ON/OFF to obtain 90°, 180° and 270° phase shift relative to the reference (0°). Measurement results show RMS phase and amplitude error equal to 10.3° and 1.2 dB, respectively. The maximum insertion loss is equal to 8.6 dB, leading to a figure of merit of 31°/dB. As shown by simulation, by flipping PIN diodes and use negative voltage for biasing, the maximum insertion loss could be reduced to 3.6 dB (figure of merit of 75°/dB) along with a great improvement in RMS phase and amplitude errors, thus showing the potential of the proposed architecture.

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In this paper, a 2-bit digital reflection-type phase shifter working at 120 GHz is presented. It uses a compact coupled-lines coupler with low insertion loss and high isolation over a wide bandwidth. The loads are made by a microstrip-line loaded by three PIN diodes whose states are tuned ON/OFF to obtain 90°, 180° and 270° phase shift relative to the reference (0°). Measurement results show RMS phase and amplitude error equal to 10.3° and 1.2 dB, respectively. The maximum insertion loss is equal to 8.6 dB, leading to a figure of merit of 31°/dB. As shown by simulation, by flipping PIN diodes and use negative voltage for biasing, the maximum insertion loss could be reduced to 3.6 dB (figure of merit of 75°/dB) along with a great improvement in RMS phase and amplitude errors, thus showing the potential of the proposed architecture.

Introduction: Since the beginning of the 2000s, the mm-waves have been explored intensively to meet the needs in terms of data rate (5G/6G for example) or spatial resolution (automotive radars, imaging). Thus, it is essential to change the way terminals and relays work to satisfy their energy requirements, which implies mastering the beams of electromagnetic waves (beamforming) to establish point-to-point communications that are energy efficient. The direction of the beams is ensured by phase shifters, which are expected to be very accurate at the phase level, with low insertion loss. In (Bi)CMOS technologies, phase shifters design is based either on an active approach, based on vector modulation using variable gain amplifiers [1] or on passive approach. The active approach allows designing circuits with a reduced footprint and very accurate phase adjustment, but it suffers from linearity issues. Conversely, the passive approach allows better control of linearity but suffers from poor compactness and high insertion loss at mm-waves, particularly above 100 GHz with the fall of the quality factor of the varactors. The passive phase shifters found in the literature all use a homogeneous principle, with either switched elements (transmission lines or filters) leading to a n-bit digital phase shifter whose complexity increases with the resolution [2], or a continuous variation of the phase (analog approach) resulting in relatively poor figures of merit (FoM), defined as the ratio of the maximum phase shift divided by the maximum insertion loss [3]. A hybrid approach as presented in [4] can allow considering the best of each approach, namely low losses for switched structures, and increased phase accuracy for analog structures. In this paper, we present a new topology of 2-bit reflection-type phase shifter (RTPS), with an operating frequency of 120 GHz, which is dedicated to be incorporated into a hybrid phase shifter. It was designed in the BiCMOS 55-nm from STMicroelectronics [5], thus benefiting of a thick back-end-of-line (BEOL). We first describe the principle of the phase shifter, then the design of the 3-dB coupler and loads. Then we describe the measurement results and show how performance could be significantly improved by simply changing the way the PIN diodes are used for switching.

Principle of 2-bit RTPS: The 2-bit RTPS architecture is shown in Fig. 1. The principle is simply based on a microstrip-line loaded by three switches (PIN diodes in Fig. 1) to create four different path lengths to get 0°, 90°, 180°, 270° digital states. The RTPS structure makes it possible to ensure very good matching over a wide frequency band.

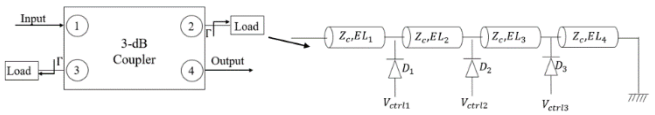
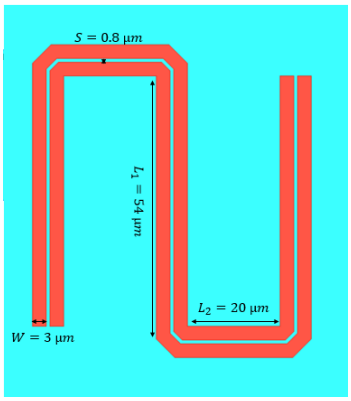
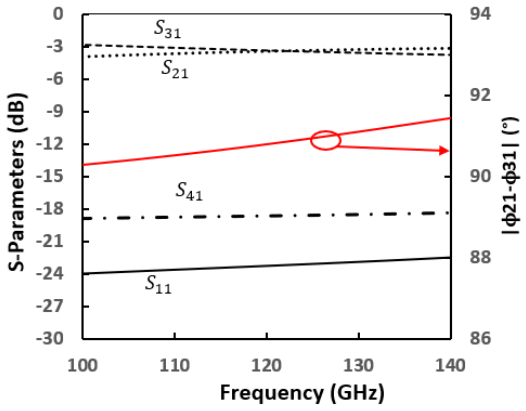


Fig. 1 *2-bit RTPS architecture.*

3-dB coupler design: A broadside coupled-lines coupler was designed, instead of a branch-line coupler, because it exhibits a wide bandwidth and can be meandered to drastically reduce its surface, as shown in Fig. 2*a*. Moreover, as compared to vertical coupled-lines couplers, it allows the use of the thicker metal layer only, with the benefit of a BEOL of maximum height, thus reducing the insertion loss. Moreover, the phse velocity of even- and odd-modes are very close, guaranteeing significant isolation. The resulting meandered coupler is very compact (67.5 x 60 µm²). The simulated S-parameters (Fig. 2*b*) show an isolation (S_{41}) better than 18 dB and a return loss (S_{11}) better than 22 dB from 100 GHz to 140 GHz. Both transmission (S_{21}) and coupling (S_{31}) parameters show insertion loss equal to 3.4 dB at 120 GHz. The phase difference between the two outputs is 90.8° at 120 GHz. Thus, the designed 3-dB coupler worked well at 120 GHz with performance that compete with the state of the art [6].



a



b

Fig. 2 *Presentation of 3-dB couple*
a Top view of the microstrip coupled lines
b Simulated S-parameters amplitude and phase against frequency

RTPS load design: The four states are defined as follows. The reference state (0°) is set by the three diodes in ON-state. Then the diode D1 is switched to OFF-state for the 90° phase shift, and the two diodes D1 and D2 are switched to OFF-state for the 180° phase shift. Finally, the 270° state is achieved when the three diodes are switched in OFF-state. Ideally, 45° electric length for each transmission line (EL2, EL3 and EL4 in Fig. 1) would provide the four digital states. However, series ON-state resistance R_{on} and OFF-state capacitance C_{off} of the basic PIN-diodes model must be considered since these parameters have a big impact on the phase shift and the amplitude of the load reflection coefficient at mm-wave frequencies. R_{on} has a big impact on the amplitude but very little on the phase shift while C_{off} mainly impacts the phase shift. Therefore, there is a trade-off for the choice of each diode to have low phase error and equal insertion loss in each state, since C_{off} and R_{on} scale inversely. The electrical lengths ELi were also modified since each transmission line is loaded by C_{off} in the OFF-state. Thus, the sizing of the PIN diodes was made in codesign with the choice of the electrical lengths ELi and the characteristic impedance of the transmission line. The other part of the design concerned the biasing of the PIN diodes. The transmission line being connected to the ground, the cathode potential is set to 0 V (Fig. 1), thus positive current (direct biasing) was used to turn the PIN diodes ON and negative voltage was used to turn the PIN diodes OFF. The PIN diodes architecture is detailed in [7]. It is a horizontal architecture with the anode (P region) in the center of two cathodes (N region). The anode uses the same P+ implantation as the source/drain of BiCMOS 55 nm

MOS transistors, while the cathode uses the N+ implantation of the HBT transistors. A Polysilicon spacer is used to define the intrinsic region I connecting the doped regions N and P. Finally, deep trenches (DTI) are made around the perimeter of the component to isolate the PIN diode from the other components. The physical parameters of the component are width intrinsic region I (W_i), anode width (W_a) and number of fingers (Nf). In this paper W_i et Nf were set to 180 nm and 8 for the 3 PIN diodes, respectively. The RTPS loads parameters obtained after optimization are given in Table 1.

Table 1: Parameters of the 2-bit RTPS load

Transmission line (Z_c in Ω & ELi in °)					PIN diodes (W_a in µm)		
Z_c	EL_1	EL_2	$EL3$	EL_4	D_1	D_2	D_3
80	10	27	40	27	2.5	1.25	3.75

Results: S-parameters measurement was performed up to 140 GHz by using an ANRITSU VectorStar® ME7838A4 VNA. An on wafer TRL calibration was performed. The 2-bit RTPS chip micrograph is displayed in Fig. 3. The surface area without pads is equal to 0.069 mm².

The S-parameters were measured for each digital state. The results are displayed in Fig. 4. The return loss is better than 14 dB from 100 GHz to 140 GHz. The phase difference for 90° and 270° states shows an acceptable phase accuracy, with phase shifts equal to -86.6° and -276.5° at 120 GHz, respectively, whereas the phase shift for the 180° state is -201.1° at 120 GHz, e.g., a phase error of 21.1°. These phase errors can be explained by the fact that the diodes model used for the design was too simple, as explained below. As a result, the RMS phase error is above 10° at 120 GHz.

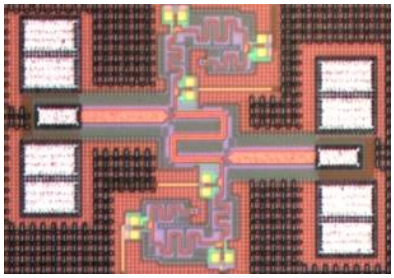


Fig. 3 *Chip microphotograph of 2-bit RTPS*

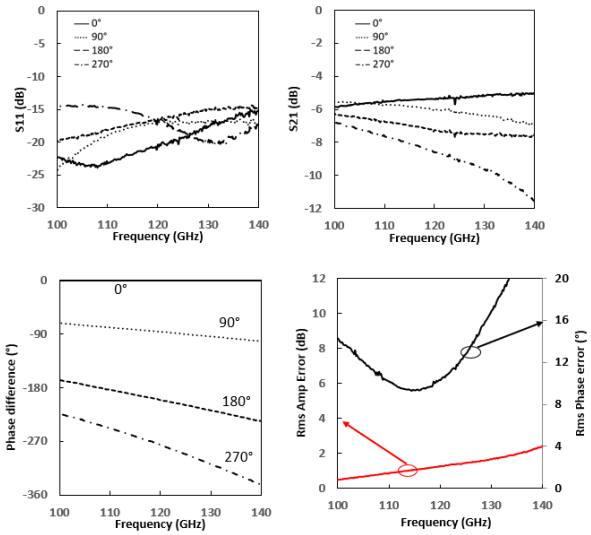


Fig. 4 *2-bit RTPS measurement results with PIN diodes modelled by resistance or capacitance.*

The lack of PIN diodes accurate electrical model has also been detrimental to insertion loss. At 120 GHz, the insertion loss is between 5.4 dB (reference 0° state) and 8.6 dB (270° state). Hence, the measurement results presented in Fig. 4 show that the working principle of the proposed 2-bit RTPS has been confirmed, but the overall performance must be improved to get acceptable performance. Thanks to the recent development of a very accurate model of the PIN diodes, especially concerning the substrate network, an optimization could be carried out after flipping the PIN diodes, leading to much better results, as shown in the next section.

Optimized design: In this section, simulation results with a much more accurate PIN diode electrical model, which was developed after the tape-out of the RTPS presented in this paper, are discussed. The most important point is related to the existence of a PN junction between the cathode and the substrate, which is modelled by a diode (D_{SUB}), and a series resistance R_s in the OFF-state (Fig. 5). D_{SUB} is always OFF; its equivalent electrical model is composed of a capacitance C_{SUB} in series with a resistance R_{SUB}. D_{SUB} is in parallel with the transmission line in the initial design (Fig. 1), thus impacting both phase shift and insertion loss. To fix this issue, the PIN diodes in Fig. 1 were flipped, so that the cathode is connected to the ground via the biasing of V_{ctrl} (see Fig. 1). A whole optimization of the load was then realized with this new configuration by considering measurements of the PIN diodes for the simulation of the 2-bit RTPS, to be as accurate as possible. The S-parameters are displayed in Fig. 6.

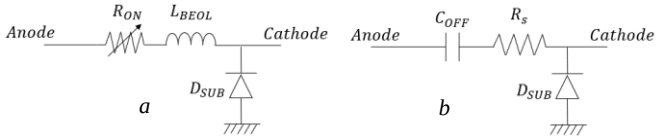


Fig. 5 *PIN diode electrical model*
a In ON-state
b In OFF-state

The insertion loss is reduced in all states, ranging between 3.3 dB and 3.8 dB at 120 GHz. As a result, RMS amplitude imbalance is reduced to 0.2 dB and stays below 1 dB on a large frequency bandwidth [86 GHz – 161 GHz]. In the same way, the RMS phase error is reduced to 0.2° at 120 GHz. The return loss is equal to 16 dB at the operating frequency. Thus, the optimized design with flipped PIN diodes permits to greatly enhance the performance of the proposed phase shifter.

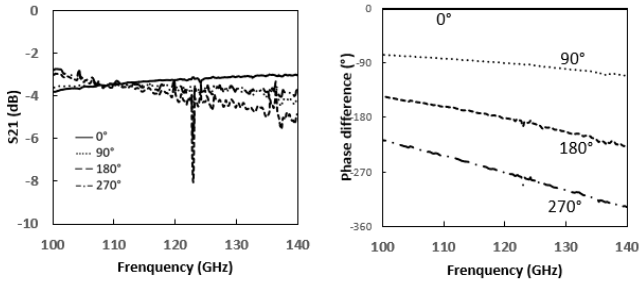


Fig. 6 *2-bit RTPS results after optimization with flipped PIN diodes*

Comparison to the state of art: The comparison to the state-of-the-art is presented in Table 2. Only the digital phase shifters with operating frequency near or above 100 GHz were considered. It is not easy to compare phase shifters with a different number of bits. In the same way it should be considered that the 2-bit RTPS presented in this paper is dedicated to being inserted within a more complex phase shifter allowing to reach either a higher number of bits, or a continuous variation of phase thanks to a hybrid approach [4]. The comparison with the state-of-the-art shows that the phase shifter presented is quite competitive in terms of insertion loss on the one hand, and phase precision on the other hand. In addition, it presents a very competitive surface.

Conclusion: In this paper, we presented a 2-bit phase shifter based on an RTPS type structure using a transmission line loaded by switches made using PIN diodes. Thanks to the use of a very compact and high-performance coupled-line coupler, the performance obtained is quite acceptable, despite inadequate use of the PIN diodes, which have not been placed in the optimal direction. Simulations based on the measurement of the PIN diodes placed in an optimal way show that the performance that can be achieved is excellent, thus validating the concept

of RTPS loaded by switched lines for the realization of passive phase shifters at mm-waves beyond 100 GHz.

Table 2: Comparison of state-of-art digital phase shifter

Reference	[2]	[8]	[9]	This work (Meas.)	This work (Simu.)
Technology	32 nm CMOS	90 nm SiGe BiCMOS	65 nm SOI	55 nm BiCMOS	55 nm BiCMOS
Freq. (GHz)	95	140	90	120	120
Ins. Loss (dB)	6.9 to 8.1	2.5 to 5.5	13	5.4 to 8.6	3.3 to 3.8
Reso. (bits)	5	4	6	2	2
RMS Ph. Err. (°)	< 6	< 13	< 2	10.2	0.2
Power (mW)	0	21	31	42.6	--
Area (mm²)	0.7	0.572	0.2	0.069	< 0.069

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References

1. Öztürk, H.J.N., Winkler, D.K.: '0.1mm2 SiGe BiCMOS Rx/Tx Channel front-ends for 120 GHz phased array radar systems', *Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2017.
2. Sayginer, G.M.R.: 'A 94-96 GHz phased-array receive front-end with 5-bit phase control and 5 dB noise figure in 32 nm CMOS SOI', *IEEE MTT-S International Microwave Symposium*, 2017.
3. M. Margalef Rovira: 'Design of mm-wave reflection-type phase shifters with oscillation-based test capabilities', PhD, Sep. 2020, p32.
4. Ferrari, R. J, Karabey, G. P. R, Maune: 'Reconfigurable circuits and technologies for smart millimeter-wave systems', Chapter 3, *Cambridge University Press*, 2022.
5. Chevalier, G. A., Ribes, A. M., *et al* :' A 55 nm triple gate oxide 9 metal layers sige bicmos technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-q millimeter-wave passives', *IEEE International Electron Devices Meeting*, pp. 3.9.1-3.9.3, 2014.
6. Rovira, J. L-A., Bautista, L. V, *et al*: 'Design of mm-wave slow-wave coupled coplanar waveguides', *IEEE T-MTT*, Vol.68, No. 12, Dec. 2020.
7. Foissey, F. G., *et al*: '85 fs Ron×Coff and CP1dB@28GHz > 25dBm innovative PIN diode integrated in 55 nm BiCMOS technology targeting mmW 5G and 6G front end module', *Silicon Monolithic Integrated Circuits in RF Systems* (*SiRF)*, 2021.
8. Rao, J.D.C.: 'A D-band reflective-type phase shifter using a SiGe PIN diode resonant load', *IEEE MWCL*, vol. 32, no. 10, Oct. 2022.
9. Zhang, K.W.: 'A 77-101GHz 6-bit vector-modulated phase shifter with low rms error in 65nm SOI CMOS', *IEEE International Conference on Integrated Circuits, Technologies and Applications, 2022.*