A novel all-digital transmitter with power equalization and harmonic elimination

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Abstract

To reduce the loss caused by power imbalance between switched-mode power amplifier (SMPA) units of all-digital transmitters (ADTx), this paper proposes an all-digital transmitter structure with power equalization and harmonic elimination. Based on the third and fifth harmonic cancellation, this structure achieves output power equalization of SMPA by controlling the width of 3-level sub-pulses to be the same. Moreover, the equalization of each switch transistor is realized by outphasing method. Finally, the feasibility of the method is verified by simulation results. For different input signals with a carrier frequency of 200 MHz, the proposed structure achieves the same output power of each SMPA unit.

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To reduce the loss caused by power imbalance between switched-mode power amplifier (SMPA) units of all-digital transmitters (ADTx), this paper proposes an all-digital transmitter structure with power equalization and harmonic elimination. Based on the third and fifth harmonic cancellation, this structure achieves output power equalization of SMPA by controlling the width of 3-level sub-pulses to be the same. Moreover, the equalization of each switch transistor is realized by outphasing method. Finally, the feasibility of the method is verified by simulation results. For different input signals with a carrier frequency of 200 MHz, the proposed structure achieves the same output power of each SMPA unit.

Introduction: With the development of high-speed switching devices, the performance of SMPA is greatly improved. Therefore, ADTx can be realized, with high-efficiency SMPA. Compared with the traditional analog transmitter, the ADTx [1]-[4] technology has flexible reconfigurability and reprogrammability. Thus, ADTx can meet the needs of software-defined radio (SDR) to achieve most of its functions in the digital domain. ADTx consist of direct digital radio frequency modulation (DDRFM), SMPA and the tunable filter. Pulse coding [5] of DDRFM is the core of ADTx to achieve high efficiency and linearity.

Radio frequency pulse width modulation (RF-PWM) [6] is one of the most suitable pulse coding algorithms for ADTx, but its implementation still has challenges. There are plenty of high-order harmonic components in the RF-PWM output pulse, which not only has higher requirements on the tuning filter but also requires the modulator and SMPA to have the ability to handle broadband signals.

SMPA is the key device for ADTx to realize power amplification in digital domain, which mainly amplifies the pulse generated by the modulator. Based on GaN based half-bridge SMPA chips [7], ADTx can synthesize and amplify the RF-PWM signal. When multiple SMPA units work at the same time, the unbalanced transmission power of GaN devices between and within SMPA units will bring additional loss and distortion [8].

To improve the coding efficiency and dynamic range, the multilevel RF-PWM scheme have been proposed [9]. This scheme can reduce harmonic distortion, but still require high Q filters to suppress harmonics. To eliminate harmonic components and relax the requirement of output filters, a 5-level RF-PWM method has been proposed [10]. The method improves the output filter bandwidth by third harmonic elimination. Based on this 5-level RF-PWM method, a multilevel RF-PWM method with the third and fifth harmonic elimination was presented [11]. The filter bandwidth was greatly improved in this scheme. To reduce the loss caused by power imbalance of the SMPA, a sub-pulse generation method was proposed [8]. The method generated two sub-pulses with equal pulse width, with the third harmonic elimination. Based on existing methods, the proposed structure with power equalization and harmonic elimination can improve the bandwidth of the filter and realize the power equalization of SMPA.

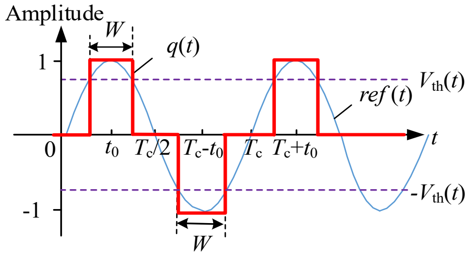

Fig 1 *Diagram of any 3-level pulse with threshold comparison*

The third and fifth harmonic elimination for multilevel RF-PWM: The multilevel RF-PWM signal can be obtained by the linear superposition of multiple 3-level pulses [10]. The normalized 3-level pulse $q(t)$ with an arbitrary period of T_c and a pulse width of W is shown in Fig. 1 where $w_c=2\pi/T_c$ is the angular frequency, and t_0 is the pulse center position. The $(2m+1)$-level RF-PWM signal can be obtained by linear superposition of m 3-level sub-pulses $q_n(t)$ (n=1, 2, ..., m), expressed as [10]:

$$p(t)=\frac{1}{m}\sum_{n=1}^{m}\sum_{k=1}^{+\infty}\frac{4\sin\left(\pi k d_n\right)}{\pi k}\cos\left[k w_c\left(t-t_n\right)\right] \quad (1)$$

where k is a positive odd number, $d_n=W_n/T_c$ is the duty cycle of the n-th 3-level sub-pulse, and t_n is the pulse center position of the n-th 3-level sub-pulse.

As the harmonic elimination conditions proposed in [11], the fundamental component of the multilevel RF-PWM signal $p(t)$ can be proportional to the input RF signal $S_{in}(t)=a(t)\cos[w_c t-\varphi(t)]$ and third and fifth harmonic components are cancelled. The pulse parameter satisfying the conditions are as follows [11]:

$$\begin{cases} \frac{1}{m}\sum_{n=1}^{m}\varepsilon_n\sin\left(\pi d_n\right)\cos\left[w_c\left(t-t_n\right)\right]=c\pi a(t)\cos\left[w_c t-\varphi(t)\right]/4 \\ \sum_{n=1}^{m}\varepsilon_n\sin\left(3\pi d_n\right)\cos\left[3w_c\left(t-t_n\right)\right]=0 \\ \sum_{n=1}^{m}\varepsilon_n\sin\left(5\pi d_n\right)\cos\left[5w_c\left(t-t_n\right)\right]=0 \end{cases} \quad (2)$$

where $\varepsilon_n=\pm 1$ is the weighting coefficient, the value is determined by the envelope amplitude $a(t)$ of the input signal, and c is the gain of the modulator.

In order to simplify the solution of (2), the simplified condition is given in [11] and eight parameter combinations are obtained. When $\Delta t_1=\Delta t_2=\Delta t$, the original RF-PWM

Table 1. Parameter groups of 3-level pulses when d_1=d_2=d_3=d_4

Parameters of sub-pulses	Simplified conditions	Parameter combination i: 1	2	3	4
Pulse position	t_1	$\varphi(t)/w_c$+ $4T_c/15$	$\varphi(t)/w_c$+ $T_c/15$	$\varphi(t)/w_c$+ $7T_c/15$	$\varphi(t)/w_c$+ $2T_c/15$
	t_2	$\varphi(t)/w_c$+ $13T_c/30$	$\varphi(t)/w_c$+ $7T_c/30$	$\varphi(t)/w_c$+ $11T_c/30$	$\varphi(t)/w_c$+ $T_c/30$
	t_3	$\varphi(t)/w_c$- $4T_c/15$	$\varphi(t)/w_c$- $T_c/15$	$\varphi(t)/w_c$- $7T_c/15$	$\varphi(t)/w_c$- $2T_c/15$
	t_4	$\varphi(t)/w_c$- $13T_c/30$	$\varphi(t)/w_c$- $7T_c/30$	$\varphi(t)/w_c$- $11T_c/30$	$\varphi(t)/w_c$- $T_c/30$
Duty-cycle	d_1=d_2=d_3=d_4	1/2-arcsin(a(t))/π			

method is obtained. The pulse width of sub-pulses in this method is different. Thus, it makes the output power of each SMPA unit different and brings power imbalance. To reduce the loss caused by power imbalance between SMPA units, the sub-pulses with d_1=d_2=d_3=d_4 in [11] is considered. Four parameter combinations of 3-level sub-pulses that satisfy the conditions of third and fifth harmonic cancellation are shown in Table 1. The 3-level sub-pulse $q_{ij}(t)$ that meets any combination in Table 1 can be generated by threshold comparison [11]. The output waveforms of combinations 1 and 2 are denoted as WI; the waveforms of combinations 3 and 4 are denoted as WII.

The power equalization method: The power equalization of SMPA units is realized by sub-pulses with the same pulse width. Under the harmonic elimination conditions, the parameters of 3-level sub-pulses with equal width are shown in Table 1. The structure of full-bridge SMPA unit which amplifies one 3-level pulse is shown in Fig. 2. The unit consists of two half-bridge SMPA chips [7] driven by 2-level pulses. As shown in Fig. 2, there are four identical switched transistors Q_1, Q_2, Q_3 and Q_4 driven by 2-level pulses S_1, S_2 and their inverse phase signals. Therefore, common threshold comparison which generates 3-level sub-pulses is not suitable for SMPA in the ADTx structure.

Therefore, the outphasing architecture is used for power equalization. As shown in Fig. 3, the outphasing method generates the 3-level sub-pulses with the same width by controlling the phase shift θ of two 2-level pulse S_1 and S_2. Taking the parameter of 3-level sub-pulse $q_1(t)$ as an example, the reference signal *ref* has same pulse position as t_1 in Table 1. The phase of S_1 and S_2 shift forward and lag behind *ref* by θ. Thus, 3-level sub-pulse $q_1(t)$=S_1+S_2. S_1 and S_2 are generated by zero-crossing comparison with $ref_1(t)$ and $ref_2(t)$ The phase shift θ, the reference signals $ref_1(t)$ and $ref_2(t)$ are expressed as:

$$\begin{cases} \theta = \arccos\left(a\left(t\right)\right) \\ ref_1\left(t\right) = \sin\left(w_c t_1 + \theta\right) \\ ref_2\left(t\right) = \sin\left(w_c t_1 - \theta\right) \end{cases} \qquad (3)$$

As shown in Fig. 3, when S_1 and S_2 is high level, Q_1 and Q_4 are the ON state; Q_2 and Q_3 are the OFF state and the output is high level. When S_1 and S_2 are low level, Q_1 and Q_4 are the OFF state; Q_2 and Q_3 are the ON state and the output is low level. When S_1 is low level and S_2 is high level or in the opposite situation, the output is zero level. Therefore, each switched transistor operates in the switch state of 50% duty-cycle, and the power equalization within and between SMPA units is both achieved.

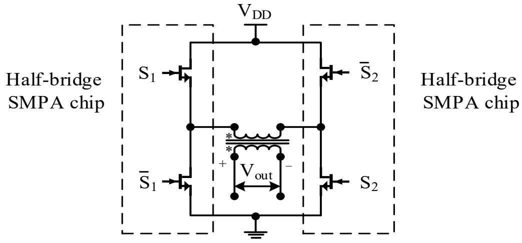

Fig 2 *The full-bridge SMPA unit structure that generates 3-level pulses*

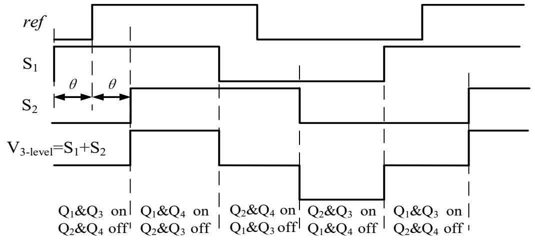

Fig 3 *Diagram of 3-level pulses generated by outphasing and the states of four switched transistor in one SMPA unit*

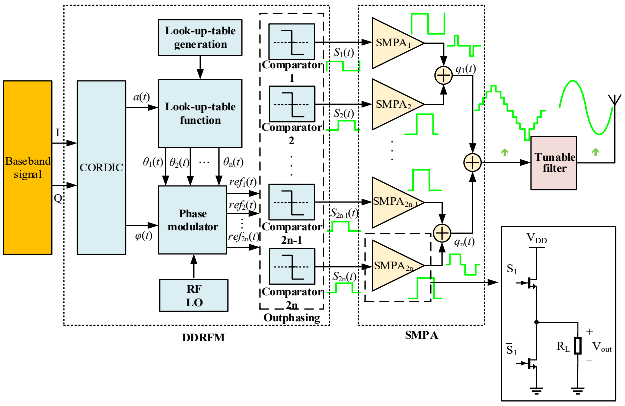

Fig 4 *Structure of RF-PWM based ADTx with half-bridge SMPA chip*

The structure of ADTx with power equalization and third and fifth harmonic elimination: As shown in Fig. 4, the baseband signal is divided into amplitude and phase through CORDIC. The outphasing architecture with zero-crossing comparators are applied to implement RF-PWM. The amplitude signal is converted to phase signal θ by the look-up table and the phase modulator generates reference signals with different phase. The comparators generate 2-level pulses to drive half-bridge SMPA chips. Therefore, the structure of ADTx can achieve power equalization and third and fifth harmonic elimination.

Simulation results and analysis: To verify the feasibility of the proposed power equalization scheme and analyze its influence on signal performance, two different methods are simulated with single tone signal and complex modulation signals as input. The original multilevel RF-PWM method in [11] is denoted as SI and the power equalization method for multilevel RF-PWM is denoted as SII.

A single-tone signal with a 200-MHz carrier is used as the input signal for different schemes. Fig. 5 and Fig. 6 show the waveforms of the sub-pulses and output RF-

PWM signals of SI and SII. The output multilevel RF-PWM signals of the two methods are both WII. Meanwhile, the width of each sub-pulse of the SII is the same, which realizes the control of the sub-pulse width and equalizes the transmission power of the SMPA.

In order to analyze the influence of variable envelope on the power equalization effect of SII, the QPSK and 16QAM signal under different peak-to-average power ratio (PAPR) with carrier frequency of 200MHz is used as input. The power of each SMPA unit in the two schemes is calculated under the load of 50Ω. Under 3.70-dB PAPR QPSK signal and 5.27-dB PAPR 16QAM signal, the power proportion of the SMPA units of the two methods is shown in Fig 7. With the increase of PAPR, the power imbalance increases between the four SMPA units in SI and the output power proportion of the high-voltage SMPA unit decreases. Meanwhile, SII achieves power equalization among four SMPA units without the influence of PAPR.

Conclusion: A novel all-digital transmitter structure with power equalization and harmonic elimination is proposed in this paper. the power equalization of the SMPA units is realized by 3-level sub-pulses with equal width. Each 3-level sub-pulse is generated by outphasing method. Meanwhile, outphasing architectures implement the equal switched time of transistors. For the 16QAM signal with a 200-MHz carrier and a 5.27-dB PAPR, the proposed method has a good suppression effect of third and fifth harmonics under the output waveform WII.

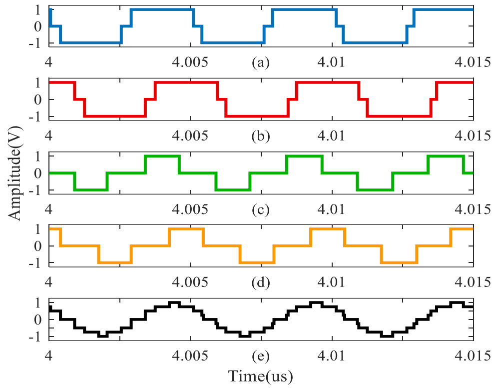

Fig 5 *Waveform of the output RF-PWM signal and four sub-pulses at a 200-MHz carrier under SI*

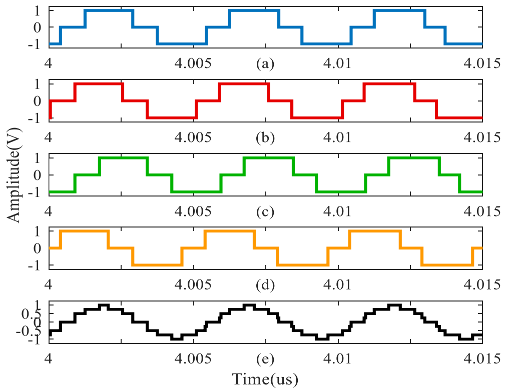

Fig 6 *Waveform of the output RF-PWM signal and four sub-pulses at a 200-MHz carrier under SII*

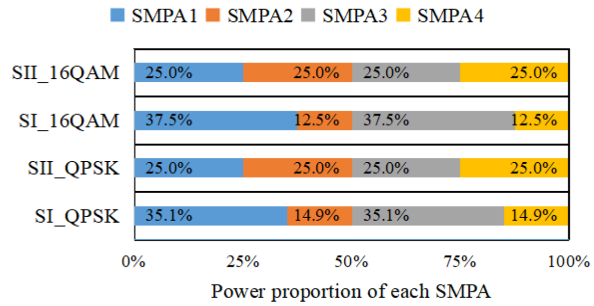

Fig 7 *The power proportion of each SMPA under SI and SII*

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