The High-Voltage Level Shifter with dV/dt noises Shielding

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Abstract

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This paper proposes a HV (high-voltage) level shifter to shield the dV/dt noise. When there is the dV/dt noises, the proposed level shifter's output is locked by the dV/dt noise shielding circuit. So, the proposed level shifter has infinite dV/dtimmunity, which is not affected by the supply voltage, and processes. In the 0.5μm BCD process, the proposed level shifter is simulated, realizing the ±250V/ns dV/dt noises shielding function and less than 1.5ns delay time under the 400V HV power supply.

Introduction: With the development of wide-bandgap power MOSFET in HV (high-voltage) applications, high-performance gate drivers are required [1-3]. HV and high-speed gate drivers are also essential in wide-bandgap power MOSFET applications due to high-frequency applications [1]. At the same time, for wide-bandgap power MOSFET's driving circuit, the synchronous gate driver is often designed on the chip to improve the system efficiency [1]. However, the largedV/dt noise generated by power devices could introduce and interfere with the synchronous gate driver. Therefore, as the critical sub-block of gate drivers, the level shifter has a high dV/dtimmunity requirement in wide-bandgap applications. The existing HV level shifters use many design techniques to improve dV/dt immunity [1-4]. These level shifters' dV/dt noise immunity has been significantly enhanced, about hundreds of V/ns. In [3], a 200V/nsdV/dt noise immunity is achieved using the capacitive level shifter in the SOI process with a 200V power supply, which is limited by the process. For most level shifters in conventional processes, thedV/dt noise has a greater influence on the level shifter with the increase of supply voltage. Then, circuits that have been to enhancedV/dt immunity and need more energy to suppress dV/dtnoise. Therefore, the existing design methods to improve level shifter immunity could gradually become unavailable with the increase of power supply voltage. This paper proposes the HV floating level shifter withdV/dt noises shielding function. The core mechanism is that whendV/dt noise occurs, the proposed level shifter locks the output to prevent it from triggering by mistake.

The dV/dt noise interference to HV level shifters: There are two situations for the HV floating level shifter disturbed by dV/dtnoises. The HV floating power supply rail rises synchronously, which is the positive dV/dt noise; the other is that the HV floating power supply rail falls synchronously, which is the negative

*dV/dt*noise. Therefore, only the circuit connected with both HV and LV regions needs to be considered when the level shifter is disturbed by*dV/dt* noises, as described in [4]. For the HV floating level shifter, HV and LV regions have the same power supply rail voltage [4]. VDDH-VSSH is equal to VDDL-VSSL, and the LV power supply rail (VDDL-VSSL) is fixed.

Fig. 1 The positive dV/dt noise interference.

Fig. 2 *The negative dV/dt noise interference.*

When IN is high, the level shifter is interfered with by the positive*dV/dt* noise, as shown in Fig. 1. When IN is high, V_A is equal to VSSH, and V_B is equal to VDDH. When the positive *dV/dt* noise comes, VSSH and VDDH rise synchronously, and nodes A and B also increase due to parasitic capacitance charging. The parasitic capacitance charging current is limited, so the rising speed of nodes A and B are relatively slow, especially for the level shifter without the *dV/dt* immunity improving circuit. Thus, V_A-VSSH and V_B-VSSH could decrease when the positive *dV/dt*noise happens. Owing to M7's body diode, V_A-VSSH could be clamped down to -V_F. The high-level V_B-VSSH may become a low-level signal and clamped to -V_F due to M8's body diode, as shown in Fig. 1(b). V_F is the forward voltage of MOSFET's body diode.

When the negative *dV/dt* noise occurs, both V_A-VSSH and V_B-VSSH could increase, as shown in Fig. 2. The analysis is similar to the above. When IN is high, and the negative *dV/dt* noise occurs, nodes A and B become high. Of course, each node voltage is within the allowed range due to the MOSFET's parasitic diode.

The proposed level shifter with dV/dt noises shielding: According to the above *dV/dt* noise interference analysis, when IN is high and VSSH and VDDH rise synchronously, both V_A-VSSH and V_B-VSSH have an undershoot. Nodes A and B could become low. When IN is high and VSSH and VDDH fall synchronously, both V_A-VSSH and V_B-VSSH have an overshot. Nodes A and B could become high. When there is no *dV/dt* noise, V_A and V_B are opposite. For example, IN is high, node A is low, and node B is high. Therefore, nodes A and B have different voltage changes in normal operation and *dV/dt*noises interference. Utilizing the differences analyzed above, the level shifter with *dV/dt* noises shielding function is proposed, as shown in Fig. 3.

The proposed level shifter's transient operating is illustrated through a low-to-high operation. When IN goes high, M1 and M3 are turned on, and M2 and M4 are turned off. Nodes A and C start going down. Then, node A's falling edge is sampled, and M_{H1} is turned on to accelerate node B's rising. After node A drops, NAND2 outputs a high signal R. At this time, node A is low and INV1 outputs a high signal. When node B is higher than the NAND1's triggering voltage, NAND1 outputs a low-level signal S. Finally, Latch outputs a high signal OUT. This is the low-to-high transient operation of the proposed level shifter, as shown in Fig. 4 (a). The high-to-low transient operation of the proposed level shifter is similar to the above operation.

As can be seen in Fig. 3 and Fig. 4 (a), when IN is high, due to the huge pull-down ability of M1 and M3, node A drops rapidly, while node B rises slowly. Therefore, the auxiliary pull-up transistors M_{H1} and M_{H2} are added to improve the proposed level shifter's response speed, as shown in Fig. 3.

The proposed level shifter can shield the *dV/dt* noise using logic gates (INV1/INV2 and NAND1/NAND2). According to the above analysis, only when the voltages of nodes A and B are different, S or R of Latch could become low. That is, the proposed level shifter starts to transfer the input signal IN to the output signal OUT. When the *dV/dt* noise occurs, nodes A and B have the same voltage variation trend. When the*dV/dt* noise is small, the voltage variation of nodes A and B cannot be higher than the logic gate's trigger voltage. Then, the output of NAND1 and NAND2 remains unchanged and OUT also keeps constant. When the *dV/dt* noise is large, the voltage variation of nodes A and B is higher than the logic gate's trigger voltage. At this time, nodes A and B have the same variation. Due to using INV1/INV2, NAND1/NAND2 could output a high signal, and the output of Latch remains unchanged. So, the output OUT of the proposed level shifter remains constant and is not disturbed by *dV/dt* noise.

Fig. 3 The proposed level shifter with dV/dt noise shielding function.

Fig. 4 The waveform of the proposed level shifter, (a) the low-to-high operation, (b) dV/dt noises shielding function when IN is high.

For example, Fig. 4 (b) shows the proposed level shifter's waveform during shielding positive and negative dV/dt noises. When IN is high, V_A-VSSH is low and V_B-VSSH is equal to VDDL. When the negative dV/dt noise comes, V_A-VSSH and V_B-VSSH rise. V_B-VSSH does not exceed VDDL+V_F due to the M8's body diode. In this situation, V_B-VSSH is always higher than the INV2's triggering voltage and $V_R$also keeps high. The variation voltage of V_A-VSSH is ΔV_A. When ΔV_A is lower than INV1's triggering voltage, V_S remains low. Then, OUT is still high. When ΔV_A exceeds the INV1's triggering, V_S becomes high. Two inputs of Latch are high, so OUT remain high. When the positive dV/dt noise comes, the operation is similar to the above.

Therefore, when IN is high, the proposed level shifter's output OUT always remains unchanged whether any dV/dt noises happens. Then, the proposed level shifter realizes the dV/dt noise shielding function. When IN is low, a similar situation also happens. Therefore, the proposed level shifter detects nodes A and B's voltage variation by logic gates INV1/INV2 and NAND1/NAND2 to determine whether there are large dV/dt noises. The proposed level shifter can shield thedV/dt noise from disturbing the output OUT.

The proposed level shifter is simulated under a 0.5μm BCD process. VSSH is 400V, and VDDL is 5V. Fig. 5 simulates the proposed level shifter'sdV/dt noise shielding function at the ±250V/ns dV/dtnoise. The simulation result shows that nodes A and B have the same voltage variation due to dV/dt noise, while input signals S and R of Latch only appear high. Therefore, the proposed level shifter's output OUT could not be disturbed by dV/dt noises. This can illustrate that the proposed level shifter has a shielding function todV/dt noise, which is also suitable for other power supply voltages and processes. Fig. 6 is the simulation result of the proposed level shifter's rising and falling delay, realizing a 1ns rising and 1.4ns falling delay time under a 400V power supply.

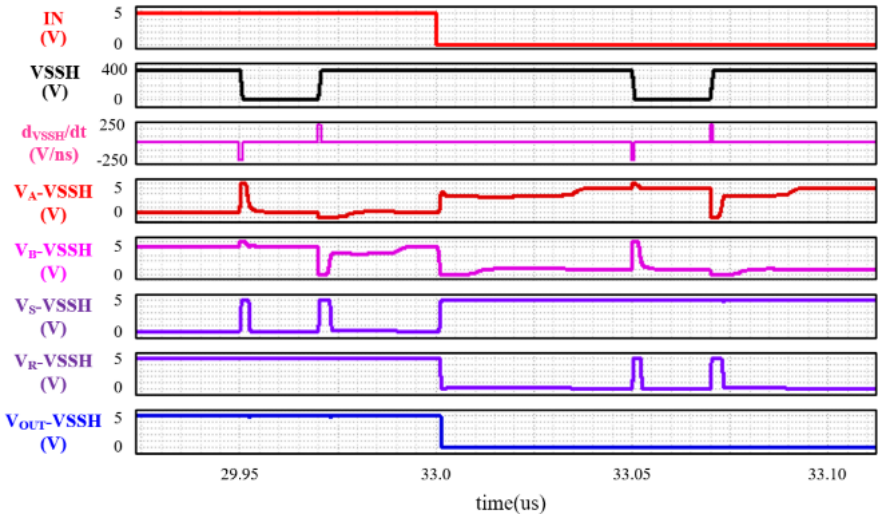

Fig.5 Simulation results of dV/dt noise immunity.

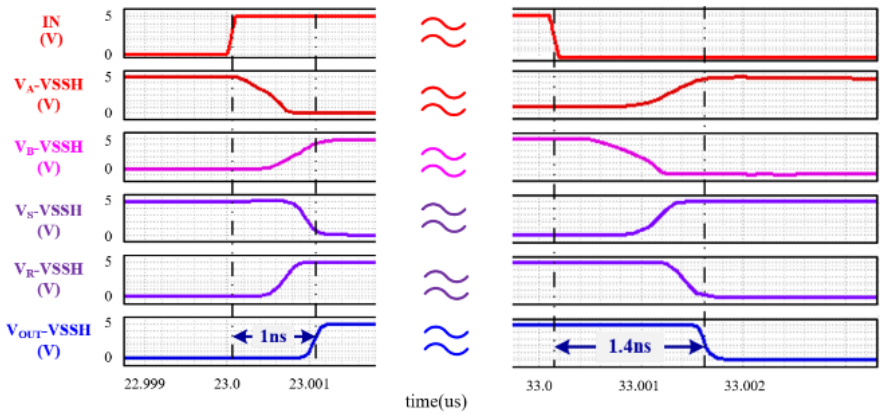

Fig.6 Simulation results of delay time.

Table 1. Comparison of HV Level shifters.

	[1]	[3]	[4]	This Work
Year	2019	2021	2021	2022
Process	0.18μm CMOS	0.18μm SOI	0.5μm BCD	0.5μm BCD
Voltage (V)	50	200	30	400
+ Slew rate (dV/dt)	200	200	250	[?]
-Slew rate (dV/dt)	[?]	200	[?]	[?]
Delay (ns)	0.53	0.67	0.66	1.2
[a]FOM	0.058	0.019	0.044	0.006

[a] *FOM from [1]: ns/(um.V).*

Table 1 shows the comparison of HV level shifters. In [1] and [4], the large positive dV/dt immunity and infinite negativedV/dt immunity are achieved under tens of voltages supply voltage. As the power supply voltage increases, dV/dt noise interference also gradually increases. Then, dV/dt immunity technologies applied in the LV field is no longer applicable. In [3], the HV level shifter realizes the 200V/ns dV/dt immunity under a 200V power supply. However, the special process, SOI process, is used in [3]. In this paper, the proposed level shifter can shield both positive and negative dV/dt noise, and infinite dV/dtimmunity, which is not influenced by processes and power supply voltages. At the same time, FOM is used to evaluate the HV level shifter's response speed. In Table I, the proposed HV level shifter has the smallest FOM. Therefore, the proposed level shifter can still achieve the enough response speed under the 400V power supply.

Conclusion: This paper proposes the HV level shifter withdV/dt noises shielding function. The dV/dt noise is shielded by logic gates without the use of complex auxiliary circuits. Therefore, the proposed level shifter's dV/dt noise immunity tends to infinity and is not affected by the supply voltage and process size. Simulation results of dV/dt immunity and delay time are implemented in a 0.5μm BCD process, realizing the dV/dt noise shielding function and no more than 1.5ns delay time under a 400V power supply. The proposed level shifter solves the problem that the supply voltage and process sizes could weaken the existing technologies to improve dV/dt immunity.

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